### Harmonics in Grid-Connected Converters: challenges and cost-effective opportunities in ASD systems

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Innovationsfonden



### **New Harmonic Reduction Techniques for Motor Drives (NHTD)**

NHTD has two work-packages based on the harmonic mitigation techniques and solutions as follows:

- **1-** *Single Drive Systems*
- 2- Multi Drive Systems

MAY 2014 → APRIL 2017

### **NHTD Team**



## Outline

Introduction (three-phase diode front-end)
 Electronic Inductor (EI) Concept
 Proposed Selective Harmonic Mitigation
 Multi-Drive Systems
 Experimental Results
 Conclusion

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## Introduction

Three-Phase Diode \_\_\_\_\_ Front-End System



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**Typical ASD System** 

#### Passive Filtering Solution



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- AC or DC side passive filtering (inductor): simple and effective to some extent. **But** they are bulky, costly, causes resonance, worsen system dynamic, and etc.
- Active harmonic mitigation solutions have been introduced to improve the input current quality. But most of them are complex, costly and reduce system efficiency.



### Typical ASD System

#### Three-Phase Diode Rectifier Passive Filtering Challenges



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Performance of three-phase diode rectification using dc-side passive filtering: (a) effect of loading condition, (b) corresponding power factor  $\lambda$  and input current THD at different power levels, (c) effect of dc-link inductor size.



### **Typical ASD System**

#### Three-Phase Diode Rectifier Passive Filtering Challenges



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Typical annual loading profile of adjustable speed drive applications: (a) water pump, (b) cooling tower.



## **Electronic Inductor Concept**

**Basic Idea** 



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### **Electronic Inductor Technique**

**Basic Concept** 



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40 30 20

> 10 0

> > 1 5 7

11 13

Harmonic No.

17 19 23 25 29 31 35 37

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- *Emulating the behavior of an ideal infinite inductor*
- THD<sub>i</sub> and Power Factor ( $\lambda$ ) independent of the load profile.
- *Controlling dc-link*  $(u_{dc})$ *.*

### **Electronic Inductor Technique**





#### No major modification is imposed to the original system!

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### **Electronic Inductor Concept**

### Load Profile



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Implementation of electronic inductor using a boost dc-dc converter topology in a three-phase diode rectifier: (a) circuit schematic, (b) corresponding input current waveform ( $i_a$ ) at different power levels. (Simulation parameters: rms line-to-line voltage  $U_{g,LL,rms}$  = 400 V, grid frequency  $f_g$  = 50 Hz, grid impedance  $L_g$  = 0.18 mH,  $R_g$  = 0.1 $\Omega$ , rated power  $P_{o,max}$  = 7.5 kW,  $U_{dc}$  = 700V,  $f_{sw}$  = 40 kHz, dc-link capacitance  $C_{dc}$  = 470 µF, and dc-link inductance  $L_{dc0}$  = 2 mH.)



### **Experimental Setup**





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System Specifications

U <sub>g,LL,rms</sub>	$f_{ m g}$	$L_{ m g}$ , $R_{ m g}$	P <sub>omax</sub> (100%)	U <sub>dc</sub>	$f_{ m sw}$	L <sub>dc0</sub>	C <sub>dc</sub>
400 V	50 Hz	0.18mH , 0.1 Ω	7.5 kW	700 Vdc	20 kHz	1 mH	470 μF

#### **Employed components**

Module	Part-Number
Three-phase diode rectifier	SKD30
IGBT-diode	SK60GAL125
IGBT gate drive	Skyper 32-pro
Controller	TMS320F28335

### **Experimental Results**

#### Original Drive (Passive Filter)

THD<sub>i</sub> = 48.7%,  $\lambda$  = 0.89 *L* = 2.5mH



 $P_o = 5kW$   $U_{dc} = 534V$ 

THD<sub>i</sub> = 67.6%,  $\lambda$  = 0.81 *L* = 2.5mH



 $P_o = 3kW$   $U_{dc} = 534V$ 

#### EI (flat current modulation)

THD<sub>i</sub> = 28%,  $\lambda$  = 0.95 *L* = 1mH, *f*<sub>sw</sub> = 20 kHz





 $P_o = 3kW$   $U_{dc} = 700V$ 



## **Improving Efficiency**

Adjustable Switching **Frequency Scheme** 

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#### Adjustable Switching Frequency



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[1] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "Energy Saving in Three-Phase Diode Rectifiers using Adjustable Switching Frequency Modulation Scheme," *EPE-2016*.

#### **Adjustable Switching Frequency**



ASFM Using strategy efficiency improves from 315W losses to 173W losses (95.8% vs 97.7%)



#### **System Specs:**

Parameter	Symbol	Value
Grid phase voltage	V <sub>abc</sub>	230 Vrms
Grid frequency	$f_{g}$	50 Hz
Grid impedance	$L_{ m g},R_{ m g}$	0.18 mH, 0.1 Ω
DC-link inductor	$L_{\rm dc-p}, L_{\rm dc}$	2.5 mH, 2 mH
DC-link capacitor	$C_{\rm dc}$	470 μF
DC-link voltage	$U_{ m dc-p}$ , $U_{ m dc}$	≈ 534V, 700 V
Rate power	$P_{o,max}(100\%)$	7.5 kW





T: Power switch (Transistor)

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#### Using WBG Devices



 $L_{dc} = 2 \text{ mH}$ 

 $L_{\rm dc} = 1 \text{ mH}$ 

Applying SiC power devices reduces the size of magnetic components and losses (131 W vs 173 W)



Pulse Pattern Modulation



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#### Pulse Pattern Modulation



[1] P. Davari, F. Zare, and F. Blaabjerg, "Pulse pattern modulated strategy for harmonic current components reduction in three-phase ac-dc converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3182-3192, July-Aug. 2016.

#### **Pulse Pattern Modulation**



$$2\beta + \theta = 60$$
$$30^{\circ} < \alpha_1 < 90^{\circ}, \alpha_2 = 120^{\circ} - \alpha_1$$

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Adding or subtracting phasedisplaced current levels

$$i_{1} = \frac{4}{\pi} [I_{dc1} \cos(30) + I_{dc2} \cos(\alpha_{1}) - I_{dc2} \cos(\alpha_{2})]$$

$$i_{k} = \frac{4}{k\pi} [I_{dc1} \cos(k30) + I_{dc2} \cos(k\alpha_{1}) - I_{dc2} \cos(k\alpha_{2})] = 0$$

$$i_{m} = \frac{4}{m\pi} [I_{dc1} \cos(m30) + I_{dc2} \cos(m\alpha_{1}) - I_{dc2} \cos(m\alpha_{2})] = 0$$

[1] P. Davari, F. Zare, and F. Blaabjerg, "Pulse pattern modulated strategy for harmonic current components reduction in three-phase ac-dc converters," IEEE Trans. Ind. Appl., vol. 52, no. 4, pp. 3182-3192, July-Aug. 2016.

#### Pulse Pattern Modulation

**Optimization** 

 $\begin{cases} Obj_{1} = M_{a} - |i_{g}(1)| \le L_{1} \\ Obj_{n} = \frac{|i_{g}(n)|}{|i_{g}(1)|} \le L_{n} \\ Objective Function \\ Weighting Factor \\ Where n = 6k \pm 1 \text{ with } k \text{ being } 1, 2, 3, \dots \end{cases}$ 

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$$\alpha_0 < \alpha_1 < \alpha_2 < \cdots < \alpha_m < \alpha_0 + \frac{\pi}{3}$$

Instead of fully nullifying the distortions, the harmonics could be reduced to acceptable levels by adding suitable constraints (L<sub>n</sub>).

Here,  $F_{obj}$  is formed based on a squared error with more flexibility by adding constant weight values  $(w_n)$  to each squared error function

[1] P. Davari, F. Zare, and F. Blaabjerg, "Pulse pattern modulated strategy for harmonic current components reduction in three-phase ac-dc converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 4, pp. 3182-3192, July-Aug. 2016.

### **Experimental Setup**



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### **Experimental Setup**

### Synthesis of the modulation signal



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$$\begin{aligned} \alpha_{1} < \alpha_{11} : & \alpha_{1} > \alpha_{11} : \\ & \left\{ \begin{aligned} & if(|\sin(3\omega_{0}t)| > \sin(3\beta)) \\ & i_{M} = I_{dc1} + I_{dc2} \\ & else \\ & i_{M} = I_{dc1} \end{aligned} \right. \\ & \left\{ \begin{aligned} & if(|\sin(3\omega_{0}t)| > \sin(3\beta)) \\ & i_{M} = I_{dc1} - I_{dc2} \\ & else \\ & i_{M} = I_{dc1} \end{aligned} \right. \\ & \left\{ \begin{aligned} & if(|\sin(3\omega_{0}t)| > \sin(3\beta)) \\ & i_{M} = I_{dc1} - I_{dc2} \\ & else \\ & i_{M} = I_{dc1} \end{aligned} \right.$$



### **Experimental Results**

#### ■ Harmonic Elimination [5<sup>th</sup>, 13<sup>th</sup>]

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■ Harmonic Elimination [7<sup>th</sup> and 13<sup>th</sup>]

$$P_o = 5 kW$$
  $U_{dc} = 700V$ 

$$Idc_1 = 1$$
,  $Idc_2 = 0.618$ ,  $\alpha_1 = 42^\circ$ 

5 <sup>th</sup> 7 <sup>th</sup> 11 <sup>th</sup> 13 <sup>th</sup>	n:300V/div \$10A/div 10ms/div
23.4%	THDi = 47.7% $1600 \text{ mA/div}$ $\lambda \approx 0.89$
4.7%	FFT of the grid current ( <i>i</i> <sub>a</sub> )

 $P_o = 5 kW$   $U_{dc} = 700V$ 

: :

$$Idc_1 = 1$$
,  $Idc_2 = 0.653$ ,  $\alpha_1 = 70^\circ$ 

Harmonic Mitigation	Harmonic Distribution and THD <sub>i</sub> (%)					
Strategy	i <sub>a</sub> (5)/ i <sub>a</sub> (1)	i <sub>a</sub> (7)/ i <sub>a</sub> (1)	$i_a(11)/i_a(1)$	i <sub>a</sub> (13)/ i <sub>a</sub> (1)	THD <sub>i</sub>	
7 <sup>th</sup> and 13 <sup>th</sup> harmonic cancellation	31.2	2.3	9.5	1	34	
5 <sup>th</sup> , 13 <sup>th</sup> harmonic cancellation	4.7	37.5	23.4	4	47.7	
Conventional method (square wave)	20	14	8.7	7.3	28.6	







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#### Basic Concept

In many applications it is a common practice to employ parallel connected drive units. In this situation the application demand is met using multiple modestly sized motor units rather than one single large unit.

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• Generating staircase total input current by proper combination





Zg SCR Vrec s Va  $V_{\rm os}$ dc R D  $C_{\rm dc}$  $L_{dc}$  $R_{11}$  $R_{q}$ Grid V<sub>rec\_d</sub> /od DC-DC de  $R_{L2}$  $C_{dc}$ **Diode Rectifier** 0.96 PF = 0.928 Power Factor (PF) 0.92 PF = 0.952 0.88 0.84 0.8 10 20 30 40 50 60

Firing angle  $\alpha_f(^\circ)$ 

[1] Y. Yang, P. Davari, F. Zare, and F. Blaabjerg, "A dc-link modulation scheme with phase-shifted current control for harmonic cancellation in multi-drive applications," IEEE Trans. Power Electron., vol. 31, no. 3, pp. 1837-1840, Mar. 2016.

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#### **Phase-shifted Flat Current Control**









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The new current modulation technique is applied to each DC-DC converter in order to further improve the current quality. However, it requires PLL for synchronization purpose.

[1] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "A multi-pulse pattern modulation scheme for harmonic mitigation in three-phase multi-motor drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 1, pp. 174-185, Mar. 2016.

[2] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "Predictive pulse pattern current modulation scheme for harmonic reduction in three-phase multi-drive systems", *IEEE Trans. Ind. Electron*, vol. 63, no. 9, pp. 5932-5942, Sept. 2016.



Pulse pattern current modulation ( $\alpha_f \neq 0^\circ$ )





#### Implemented Setup





#### Experimental Results (phase shift control)







 $P_{SCR} = 3 \text{ kW}, P_{DR} = 3.63 \text{kW}, U_{dc} = 700 \text{V}$ 



THD<sub>i</sub>  $\approx$  15.8%,  $\lambda$  = 0.95



 $P_{SCR} = 3 \text{ kW}, P_{DR} = 3.36 \text{kW}, U_{dc} = 700 \text{V}$ 



#### Experimental Results (current modulation)









THD<sub>i</sub>  $\approx$  8.6%,  $\lambda$  = 0.94



 $P_{SCR} = 3 \text{ kW}, P_{DR} = 3.65 \text{ kW}, U_{dc} = 700 \text{ V}$ 

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#### Extending number of the units (phase shift control)



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#### Extending number of the units (current modulation)



#### **Experimental Setup**





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# Conclusion

**b** The EI technique can significantly improve the THD<sub>i</sub>,  $\lambda$  and stable DC link

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- The proposed pulse pattern modulation can eliminate low order harmonics
- With multi-drive configuration, the EI technique can further reduce the THD<sub>i</sub>
- The EI technique can maintain the system performance under non-ideal operation conditions (e.g., unbalanced grid)
- The efficiency of EI technique can be significantly improved by employing WBG devices, alternative topologies and smart control techniques



# **Thank You**







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