PhD Public Defence

**Title:** Multidisciplinary Design Tool for Power Circuits (with focus on high power modules)

**Location:** Pontoppidanstræde 101, Room 23

**Time:** Friday 27 November 2015 at 13.00

**PhD defendant:** Amir Sajjad Bahman

**Supervisor:** Professor Frede Blaabjerg

**Moderator:** Associate Professor Dezso Sera

**Opponents:**
- Professor Claus Leth Bak, Dept. of Energy Technology, AAU (chairman)
- Professor Fabrizio Marignetti, University of Cassino and southern Lazio, Italy
- Professor Suresh Perinpanayagam, Cranfield University, UK

All are welcome. The defence will be in English.

After the public defence there will be an informal reception in Pontoppidanstræde 101 room 25/27.
Abstract:

This thesis presents multidisciplinary modelling techniques in a Design for Reliability (DFR) approach for power electronic circuits. With increasing penetration of renewable energy systems, the demand for reliable power conversion systems is becoming critical. Since a large part of electricity is processed through power electronics, highly efficient, sustainable, reliable and cost-effective power electronic devices are needed. Reliability of a product is defined as the ability to perform within its predefined functions under given conditions in a specific time. Because power electronic devices are applied in a wide range of loads and frequencies, the reliability of a power device may face to challenges to perform within the product specification in different application where high electrical/thermal stresses are undertaken by the device. Moreover, with the integration of power electronic devices in a compact package, e.g. power module, DFR approach meets trade-offs in electrical, thermal and mechanical design of the device.

Today, virtual prototyping of power electronic circuits using advanced simulation tools is becoming attractive due to cost/time saving in building potential designs. With simulations, the designer can test new concepts and optimize design layouts before the physical components and systems are built up. Moreover, if a failure occurs, there will be no destruction, but valuable data is obtained to modify and to optimize the product as part of an iterative design process. A key requirement to this process is to quickly generate compact and simple models describing the electrical and thermal performance of a potential design. Even though, numerical tools based on Finite Element Analysis (FEA) are powerful in studying the physical behavior of power devices, they are time consuming and demand for expensive computation facilities in DFR approach. Therefore, in this thesis focus is placed on the generation of accurate, simple and generic models to study and assess thermal and electrical behavior of power electronic circuits (especially power modules).

In this thesis, different power electronic converter topologies and control strategies are first investigated with focus on the identification of more efficient solutions. Several power converter topologies are discussed and compared with alternative solutions from power dissipation and efficiency point of view. Secondly, by understanding the methods gain to identify power dissipation in the power modules, FEM simulations are utilized to investigate thermal behavior of power module in normal (e.g. power cycling) as well as abnormal (e.g. short-circuit) conditions. Understanding the challenges and shortcomings in FEM simulation in reliability assessment of power modules, a three-dimensional lumped thermal network is proposed to be used for fast, accurate and detailed temperature estimation of power module in dynamic operation and different boundary conditions.

As an important issue in the reliability of power electronics is the thermal management of power devices, efficient cooling system design will be aimed in the following. Due to better performance of direct liquid cooling systems compared to forced air cooling systems, they will be utilized to cool down the power module. A design tool is presented with a user friendly environment to be used for optimization of cooling system layout with respect to thermal resistance and pressure drop reductions.
Finally, extraction of electrical parasitics in the multi-chip power modules will be investigated. As the switching frequency of power devices increases, the size of passive components are reduced considerably that leads to increase of power density and cost reduction. However, electrical parasitics become more challenging with increasing the switching frequency and paralleled chips in the integrated and denser packages. Therefore, novel electrical parasitics models are developed based on micro-strip structures to predict parasitic parameters according to varied layouts.

Some of the presented models in this thesis are verified by FEM simulations and experimental results in order to ensure the validation of models in the real world. The power loss, thermal and electrical parasitics models are generic and valid to be used in circuit simulators or any programeing software. These models are important building blocks for the reliable design process or performance assessment of power electronic circuits. The models save a lot of time and cost of power electronics designers in the evaluation of new ideas or assessment of products in normal and abnormal operations.