MMC CAPACITOR VOLTAGE BALANCING IN NEAREST LEVEL CONTROL

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Outline

➢ Introduction

➢ Sorting Methods for NLC

➢ Proposed Solutions:
  • Sorting Networks
  • Capacitor Voltage Mapping Strategy

➢ Conclusions
Structure of MMC

Advantages:
• Reduced harmonics
• High modularity
• Scalability
• Low switching losses
• High reliability
• Fault tolerance

Challenges:
• Circulating Current Control
• Loss balance among SMs
• Capacitor Voltage Balancing
• Complex control
Control scheme of MMC

Maximum Sampling Period $T_s$:

$$T_s = \frac{1}{\pi N f_1}$$

$N$ = number of SMs
$f_1$ = 50 Hz

Given data:

$T_{ex} \leq T_s$

Graph showing maximum $T_s$ vs. number of SMs $N$. The graph decreases as $N$ increases, indicating the limitation on $T_s$. The data from 14-06-2017.
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Sorting Methods for NLC

Bubble Sorting Algorithm

**Advantage:**
- Easy to implement.

**Drawbacks:**
- The execution time is not fixed and it depends on the input list.
- The execution time increases when N grows.

Max/Min Approach

**Advantage:**
- Easy to implement.
- The sorting method is avoided.
- Less execution time than Bubble sorting algorithm.

**Drawbacks:**
- If more than one SM has to be inserted, for example during faults, the max/min method needs more sampling periods to insert the required SMs. This affects the control dynamic.
Sorting Methods for NLC

Tolerance Band

**Advantage:**
- Reduced switching frequency.

**Drawbacks:**
- A sorting method is required.
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Sorting Networks

- The Sorting Networks are typically good solutions for FPGA:
  - Even-Odd Sorting Network
  - Bitonic Sorting Network
- They are faster than the sorting algorithms due to the parallel construction.

Bitonic Sorting Networks with $N = 8$

Compare & Swap Operator

Sorting Networks

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Capacitor Voltage Mapping Strategy

$V_{C_{\text{min}}}$ and $V_{C_{\text{max}}}$ are derived from the design parameters.
Capacitor Voltage Mapping Strategy

\[ \Delta V = \frac{V_{C_{\text{max}}} - V_{C_{\text{min}}}}{M} \]
Capacitor Voltage Mapping Strategy

![Diagram of capacitor voltage mapping strategy]

- $V_{C_{max}}$
- $V_{C_{min}}$
- Memory Array
- Map
- $V_{C_{min}}$ / $ΔV$
- $V_{C_i}$
- $ADD_{R_i}$
- round

14-06-2017
Capacitor Voltage Mapping Strategy

- M FIFO Memory → Voltage Resolution
- Memory depth equal to N
- The position is stored in the cell

\[
V_{C_{\text{min}}} = 14 \text{ V} \\
\Delta V = 0.5 \text{ V}
\]

Inside a voltage range the capacitor voltage values are considered to be identical
Simulation Results

**Table: MMC parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-link Voltage $V_{DC}$</td>
<td>200 kV</td>
</tr>
<tr>
<td>SM Capacitor $C$</td>
<td>36 µF</td>
</tr>
<tr>
<td>Arm Inductance $L_{arm}$</td>
<td>50 mH</td>
</tr>
<tr>
<td>Arm Resistance $R_{arm}$</td>
<td>1 Ω</td>
</tr>
<tr>
<td>Number of SM $N$</td>
<td>16</td>
</tr>
<tr>
<td>Sampling frequency $f_s$</td>
<td>10 kHz</td>
</tr>
</tbody>
</table>

**Table: grid parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid frequency $f_{grid}$</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Grid Voltage $V_{grid}$</td>
<td>121.2 kV</td>
</tr>
<tr>
<td>Grid Inductance $L_{grid}$</td>
<td>16.7 mH</td>
</tr>
<tr>
<td>Grid Resistance $R_{grid}$</td>
<td>0.52 Ω</td>
</tr>
</tbody>
</table>
HIL Results

Capacitor voltages

Circulating current

Output current

Total execution time

Switching

BSA  max/min  MCVB in PS  MCVB in PL

14-06-2017
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Conclusions

- Two solutions have been proposed for the capacitor voltage balancing algorithm:
  - Sorting Networks
  - Capacitor Voltage Mapping Strategy

- The simulation results for the CVMS have been shown.

- The HIL results have also been presented.
Thank you for your Attention

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