# MMC CAPACITOR VOLTAGE BALANCING IN NEAREST LEVEL CONTROL

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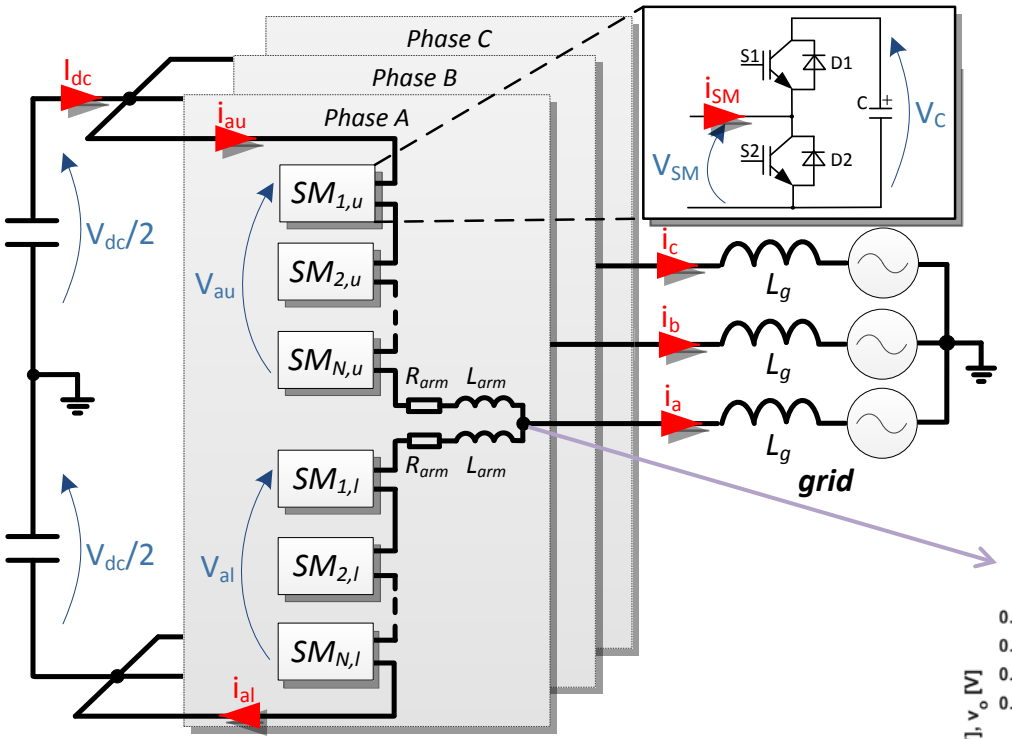
# Outline

- Introduction
- Sorting Methods for NLC
- Proposed Solutions:
  - Sorting Networks
  - Capacitor Voltage Mapping Strategy
- Conclusions

# Structure of MMC

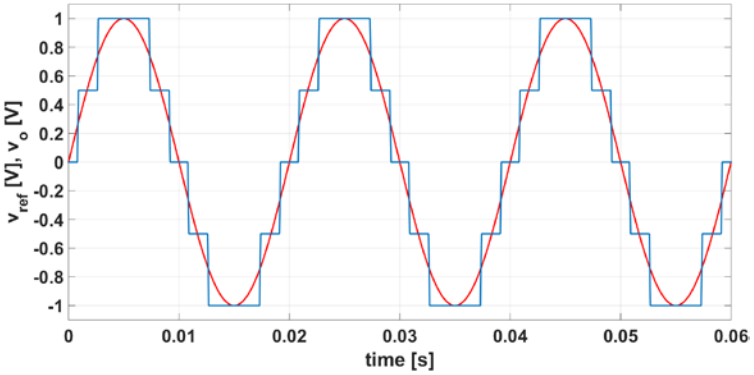



**Advantages:**

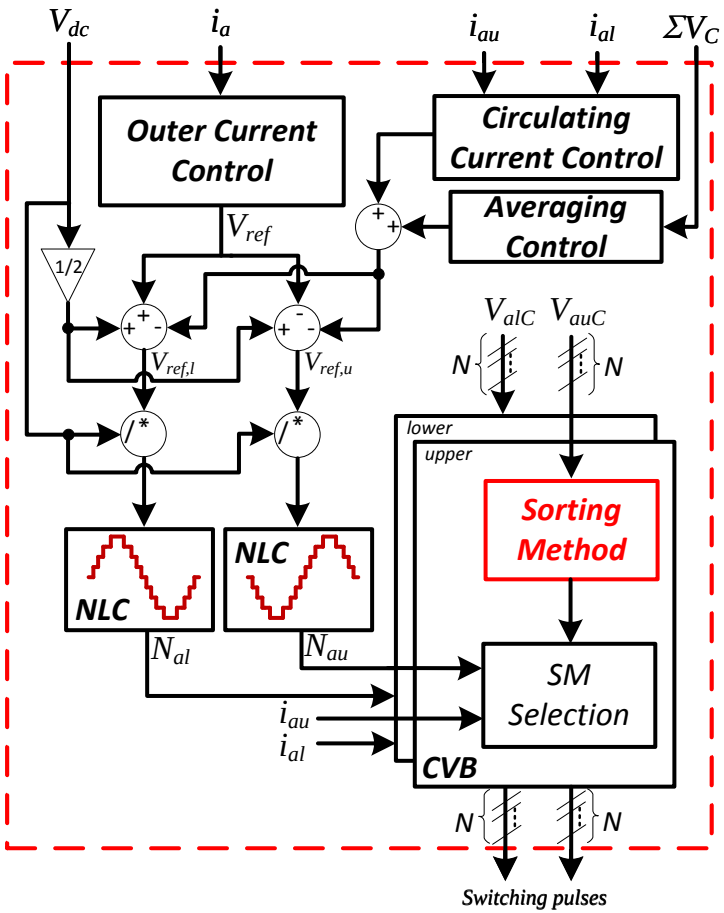
- Reduced harmonics
- High modularity
- Scalability
- Low switching losses
- High reliability
- Fault tolerance

**Challenges:**

- Circulating Current Control
- Loss balance among SMs
- Capacitor Voltage Balancing
- Complex control



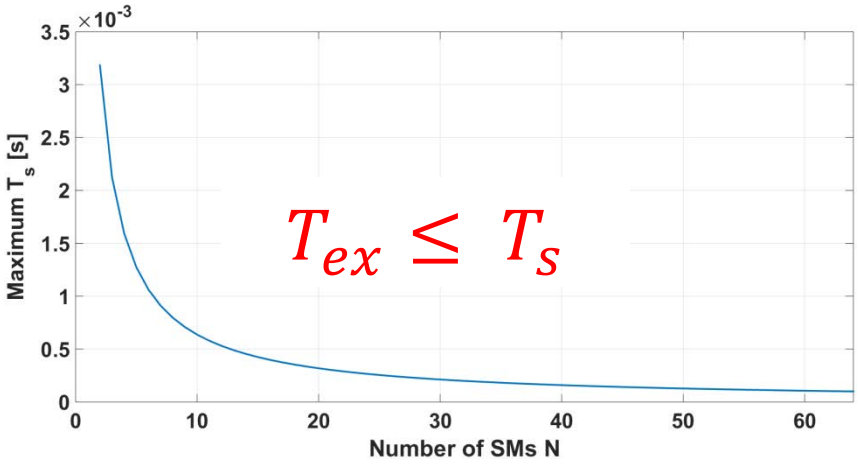
# Control scheme of MMC




Maximum Sampling Period $T_s$:

$$T_s = \frac{1}{\pi\, N\, f_1}$$

N = number of SMs
$f_1$ = 50 Hz



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# Sorting Methods for NLC

## Bubble Sorting Algorithm

**Advantage:**

- Easy to implement.

**Drawbacks:**

- The execution time is not fixed and it depends on the input list.
- The execution time increases when N grows.

## Max/Min Approach

**Advantage:**

- Easy to implement.
- The sorting method is avoided.
- Less execution time than Bubble sorting algorithm.

**Drawbacks:**

- If more than one SM has to be inserted, for example during faults, the max/min method needs more sampling periods to insert the required SMs. This affects the control dynamic.

# Sorting Methods for NLC

## Tolerance Band

**Advantage:**

- Reduced switching frequency.

**Drawbacks:**

- A sorting method is required.

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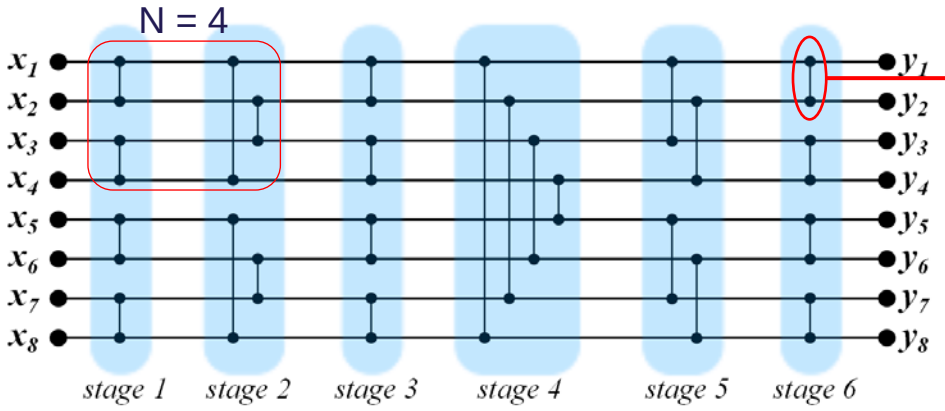
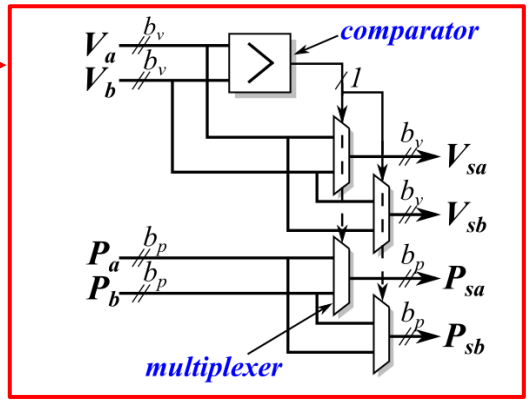
# Sorting Networks

- The Sorting Networks are typically good solutions for FPGA:
  - Even-Odd Sorting Network
  - **Bitonic Sorting Network**
- They are faster than the sorting algorithms due to the parallel construction.




Bitonic Sorting Networks with N = 8




Compare & Swap Operator

M. Ricco, L. Mathe and R. Teodorescu, "FPGA-based implementation of sorting networks in MMC applications," *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

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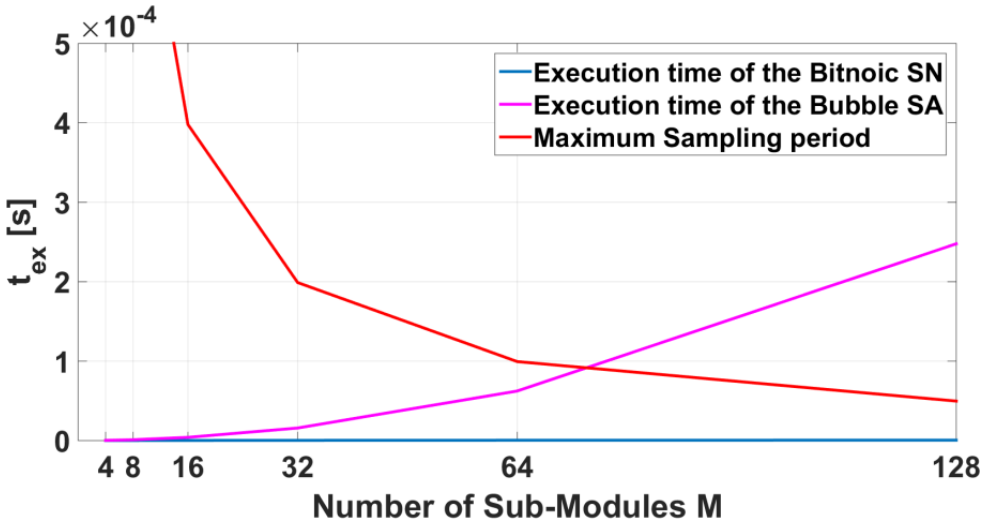


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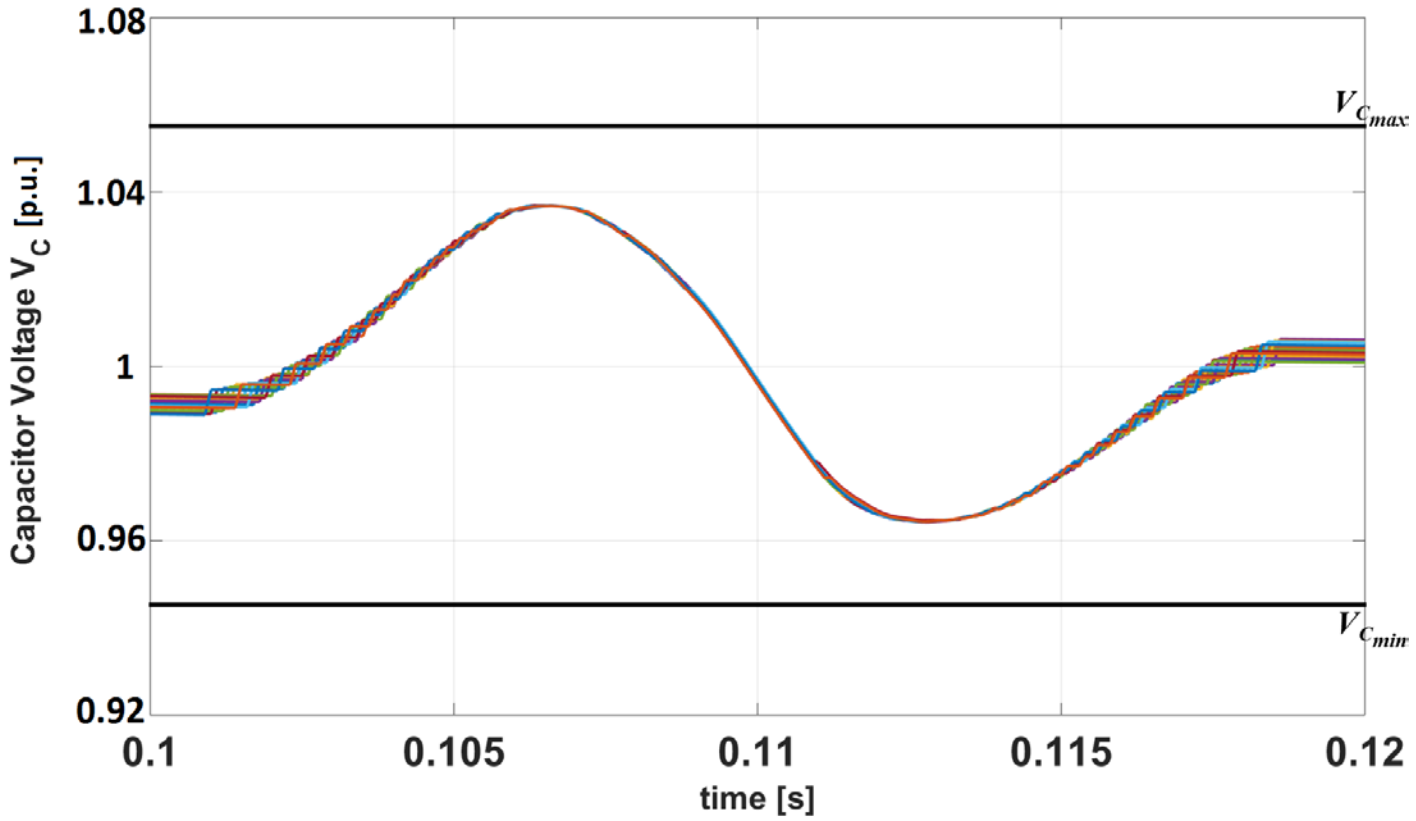
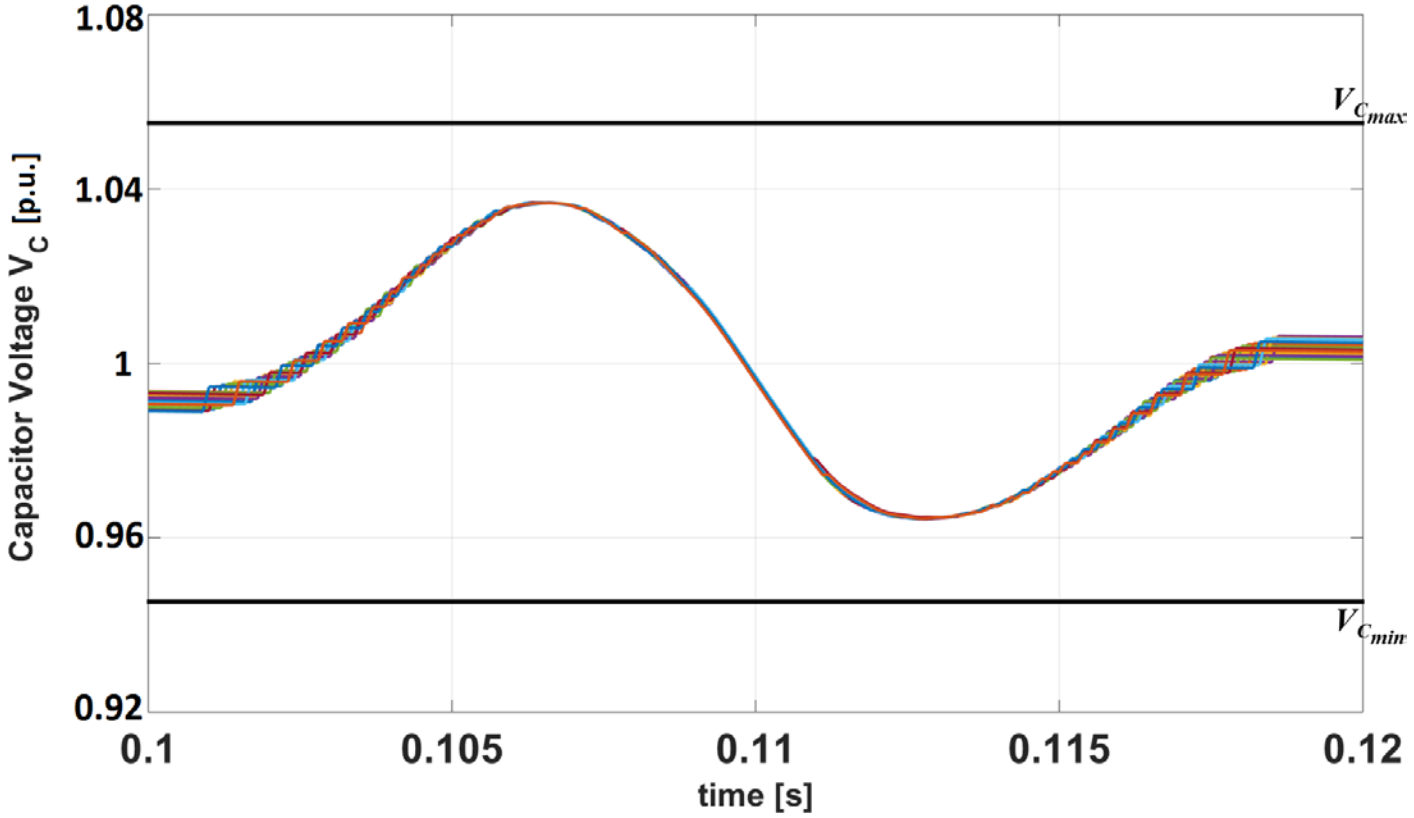
# Capacitor Voltage Mapping Strategy



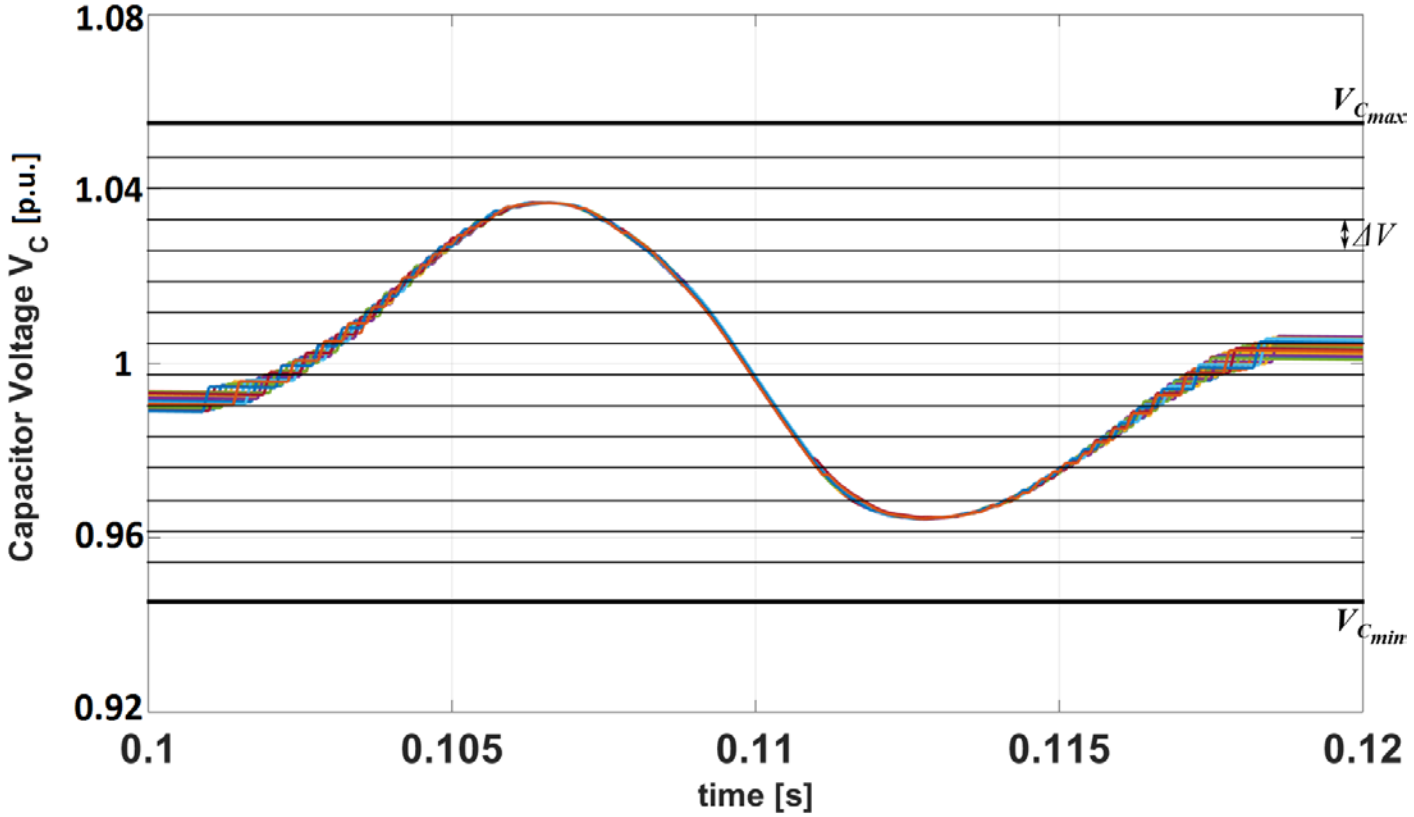

M. Ricco, L. Mathe and R. Teodorescu, "New MMC capacitor voltage balancing using sorting-less strategy in nearest level control," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

# Capacitor Voltage Mapping Strategy



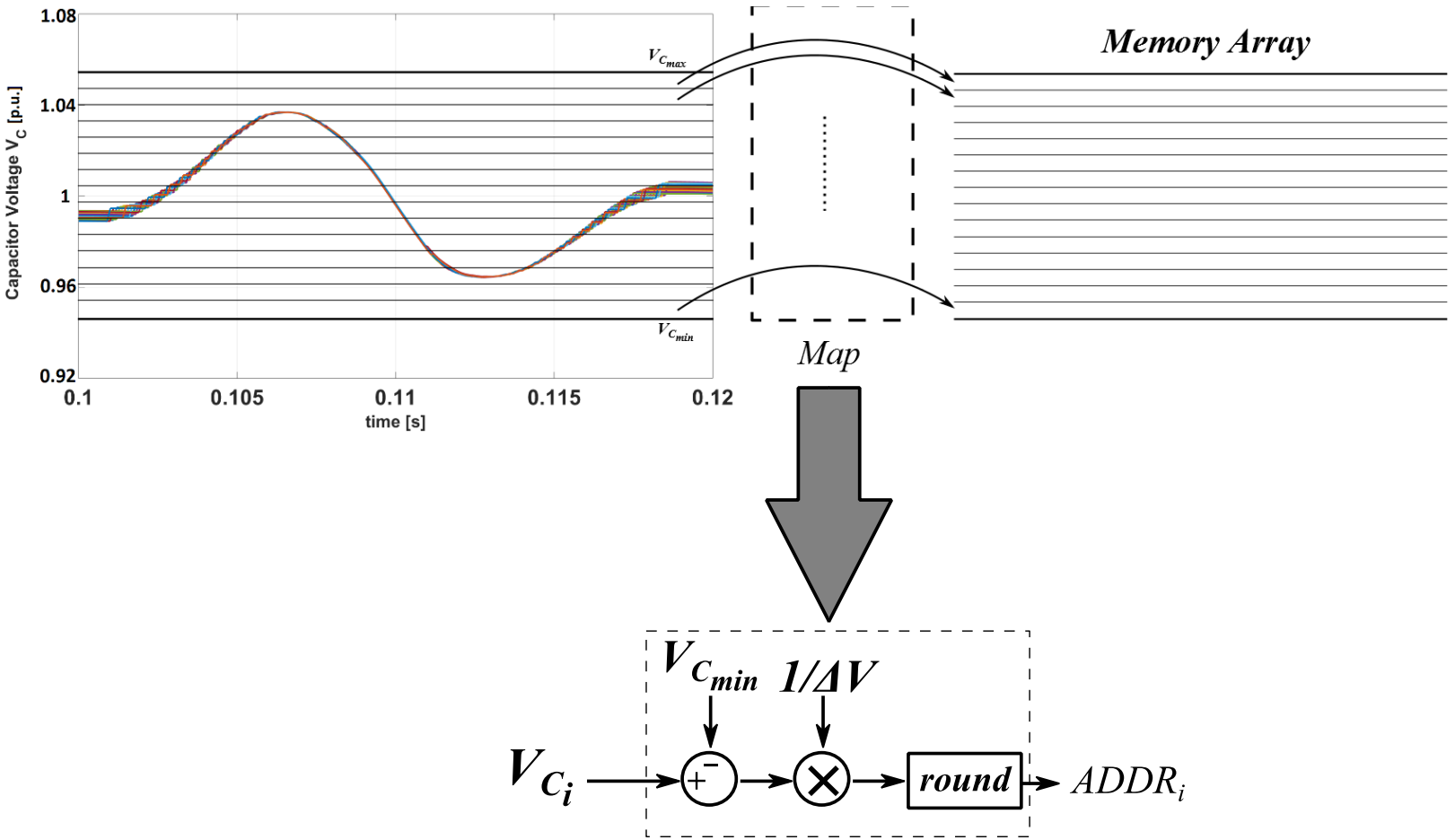

$V_{C_{min}}$ and $V_{C_{max}}$ are derived from the design parameters.

# Capacitor Voltage Mapping Strategy



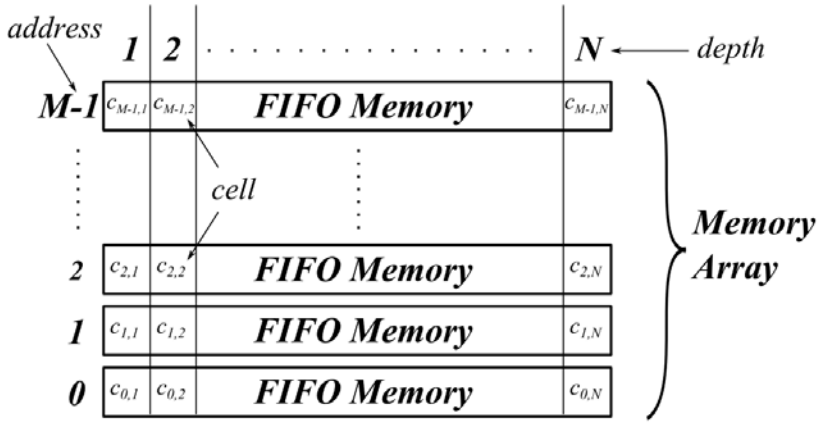

$$\Delta V = \frac{V_{C_{max}} - V_{C_{min}}}{M}$$

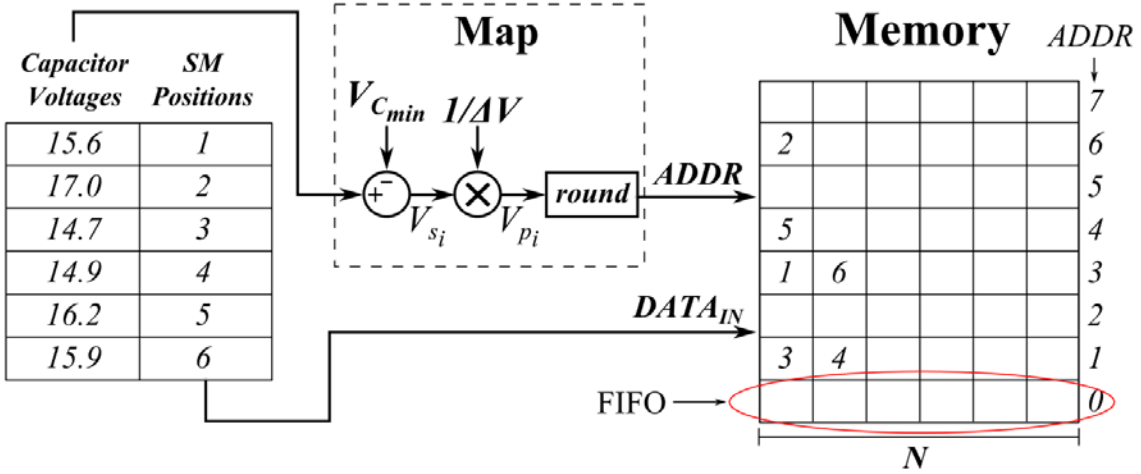
# Capacitor Voltage Mapping Strategy



# Capacitor Voltage Mapping Strategy

- M FIFO Memory → Voltage Resolution
- Memory depth equal to N
- The position is stored in the cell




$$V_{C_{min}} = 14\ V$$
$$\Delta V = 0{,}5\ V$$

- Inside a voltage range the capacitor voltage values are considered to be identical

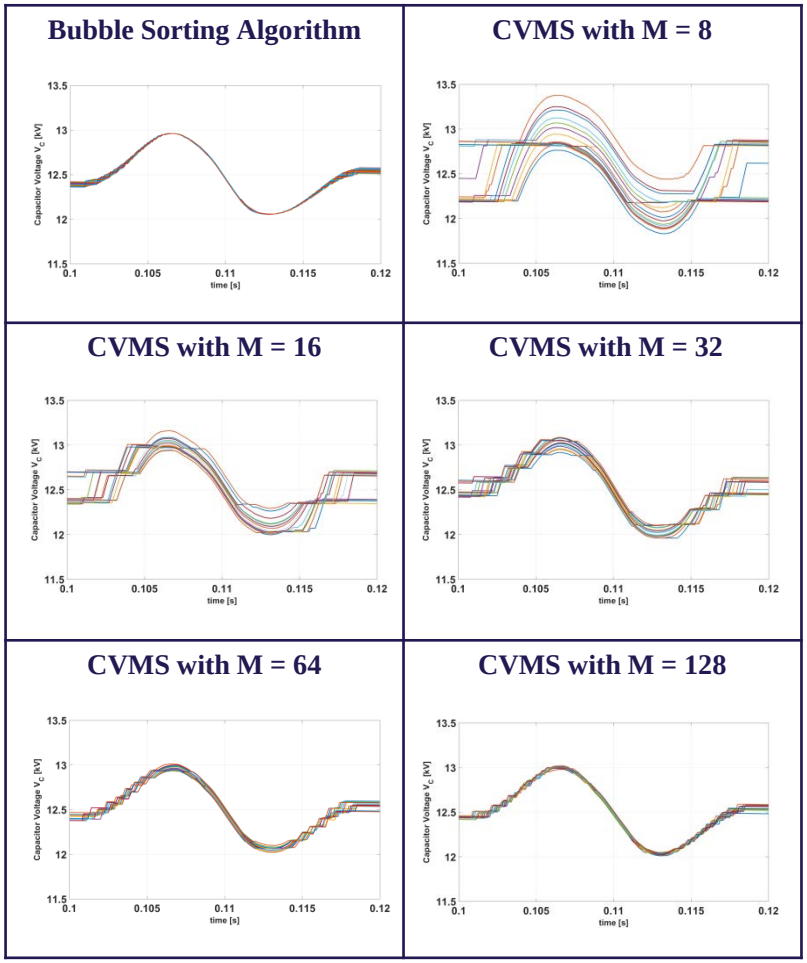
# Simulation Results

**Table: MMC parameters**

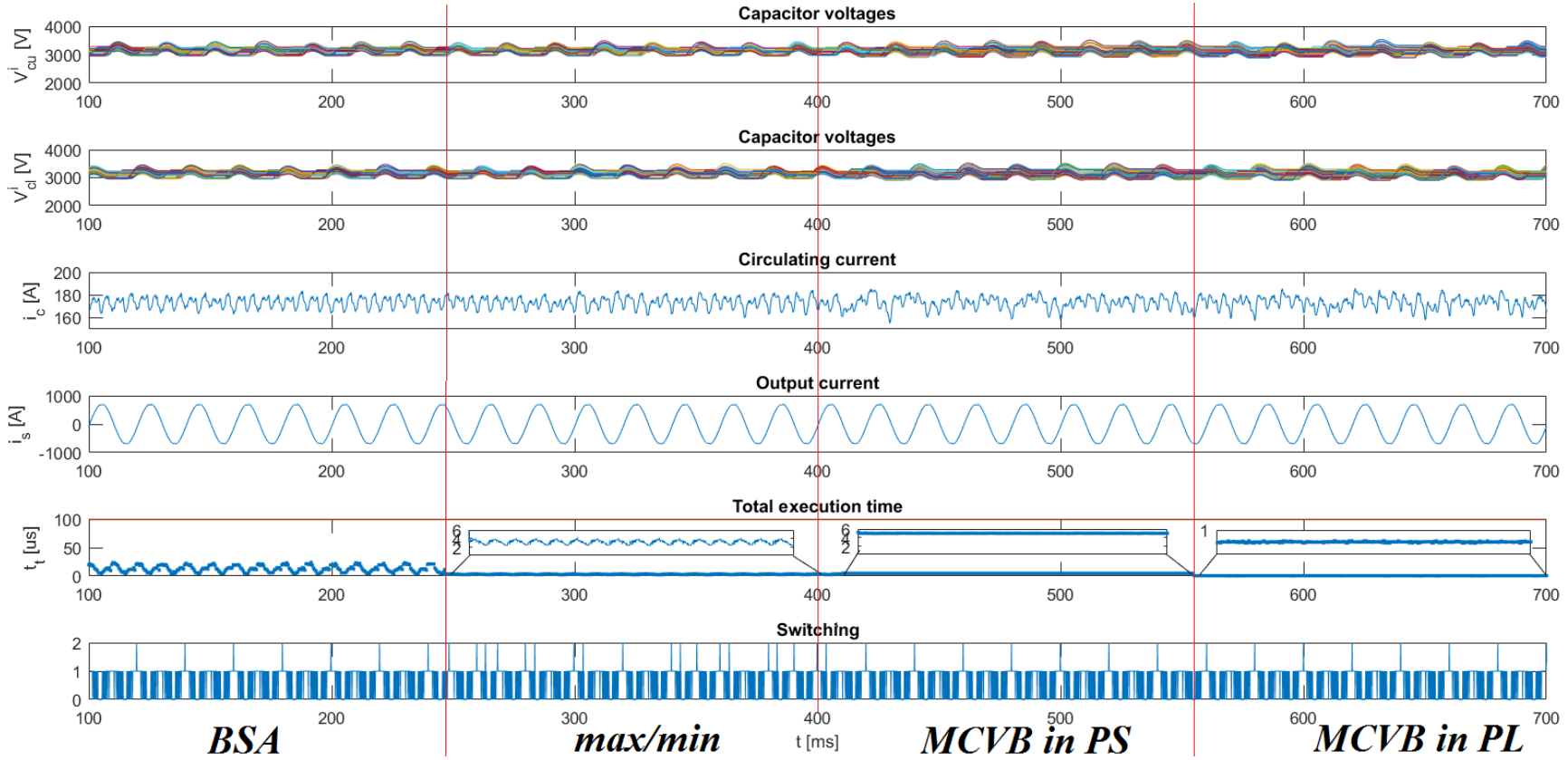
| Parameter | Value |
|---|---|
| DC-link Voltage $V_{DC}$ | 200 kV |
| SM Capacitor $C$ | 36 µF |
| Arm Inductance $L_{arm}$ | 50 mH |
| Arm Resistance $R_{arm}$ | 1 Ω |
| Number of SM $N$ | 16 |
| Sampling frequency $f_s$ | 10 kHz |

**Table: grid parameters**

| Parameter | Value |
|---|---|
| Grid frequency $f_{grid}$ | 50 Hz |
| Grid Voltage $V_{grid}$ | 121.2 kV |
| Grid Inductance $L_{grid}$ | 16.7 mH |
| Grid Resistance $R_{grid}$ | 0.52 Ω |



# HIL Results


Capacitor voltages
$V_{cu}^{i}$ [V]
Capacitor voltages
$V_{cl}^{i}$ [V]
Circulating current
$i_c$ [A]
Output current
$i_s$ [A]
Total execution time
$t_t$ [us]
Switching
t [ms]
BSA
max/min
MCVB in PS
MCVB in PL

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# Conclusions

- Two solutions have been proposed for the capacitor voltage balancing algorithm:
  - Sorting Networks
  - Capacitor Voltage Mapping Strategy
- The simulation results for the CVMS have been shown.
- The HIL results have also been presented.

# Thank you for your Attention

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