Modeling and Simulation of Complex Converters

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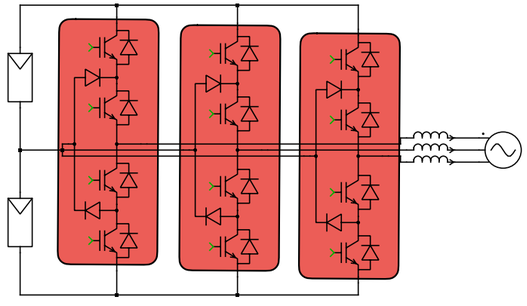
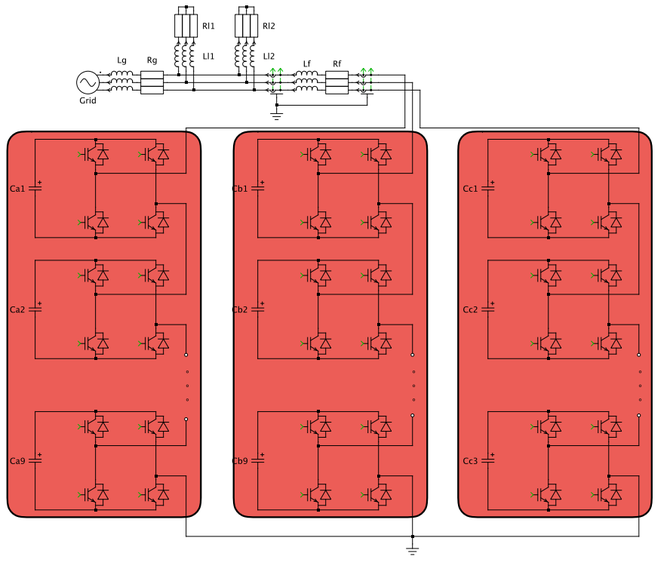
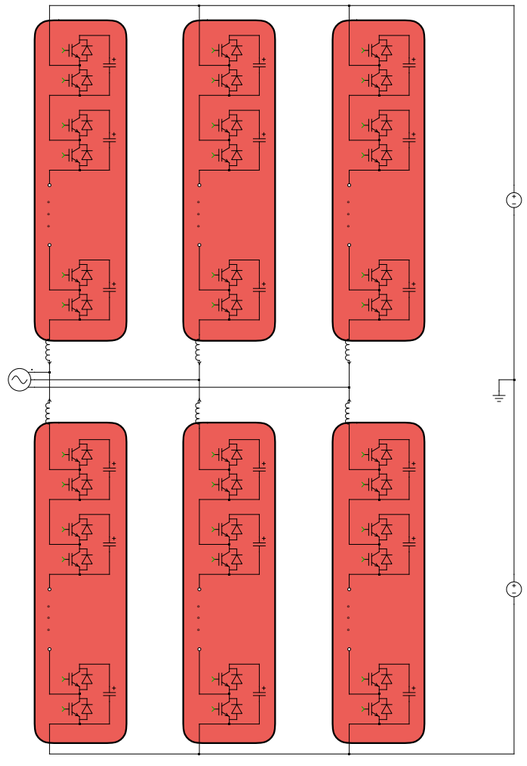
electrical engineering software

Motivation

- Converters in MV/HV grids have complex topologies
  - Voltage and current rating of switching devices
  - Harmonic requirements
- Large amount of components
  - Result in large model size
  - Multiple instances needed







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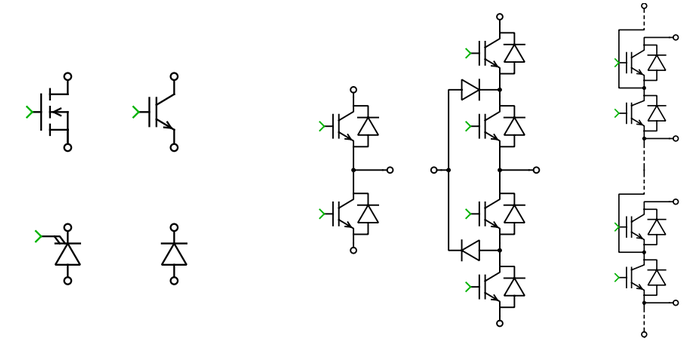
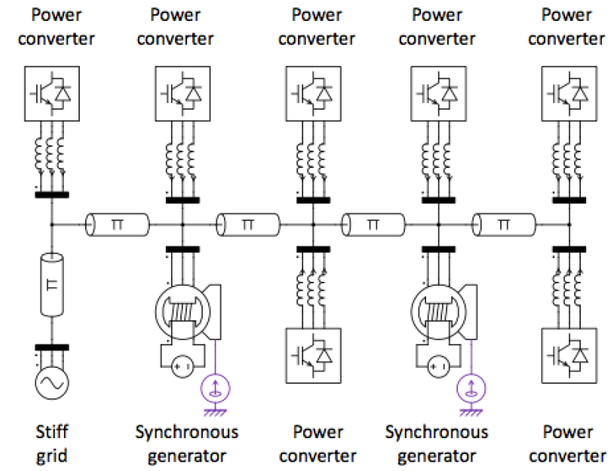
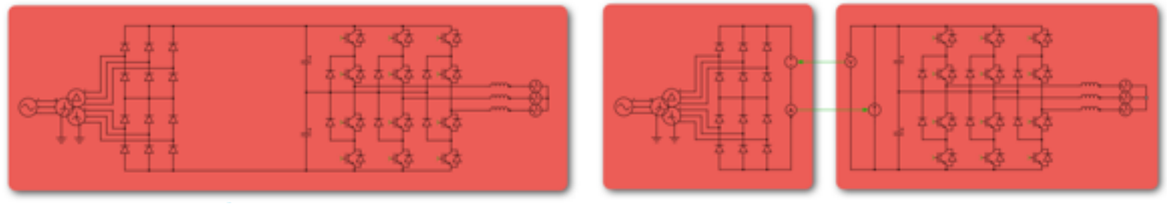


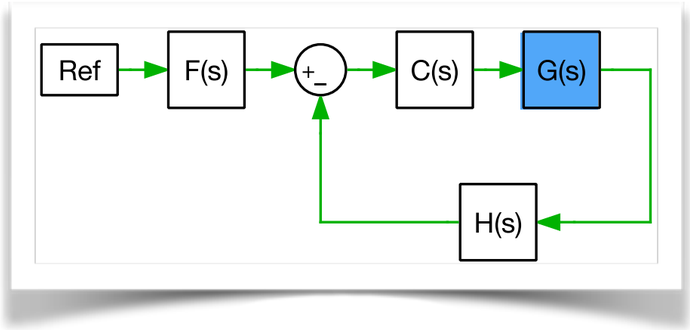




Model of Switching Devices - Level of Details

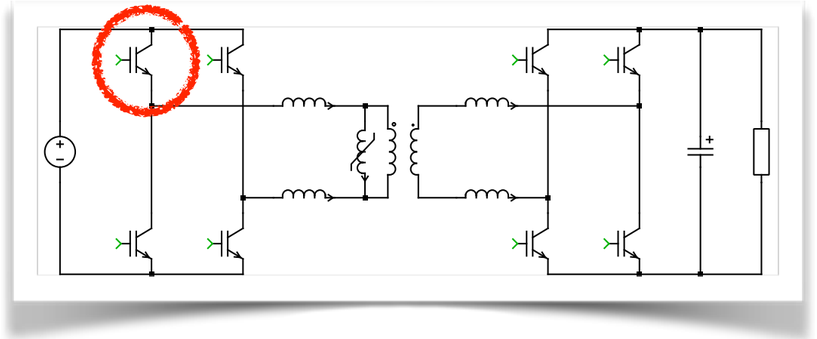
Linear transfer function

- Small-signal behaviour
- No switching, no harmonics
- Controller design



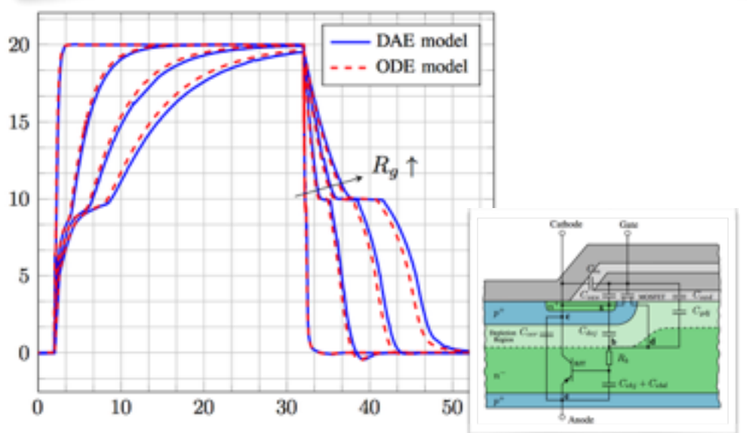
Circuit with simplified components

- Large-signal behaviour, voltage and current waveforms
- **Including switching ripples**
- Circuit design and controller verification



Circuit with specific components

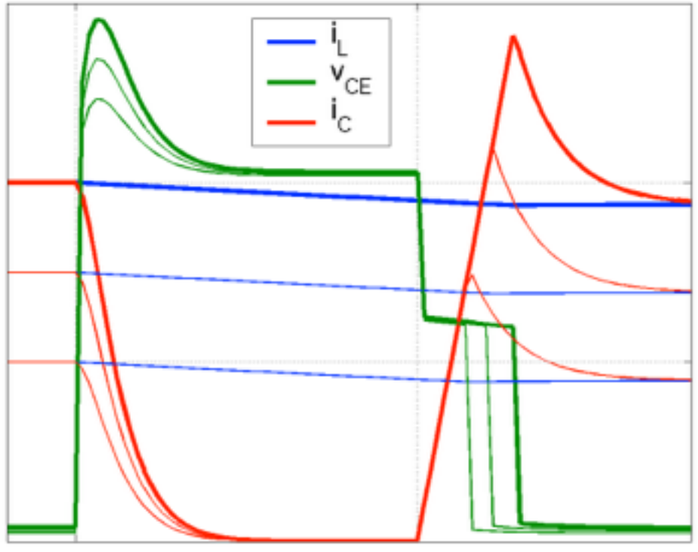
- Switching transitions (di/dt,dv/dt)
- Component stress (electrical overshoot or thermal loss)
- Parasitic effects (stray inductance)
- Optimization of components



Model of Switching Devices - Behavioral Model

Spice-type behavioural model

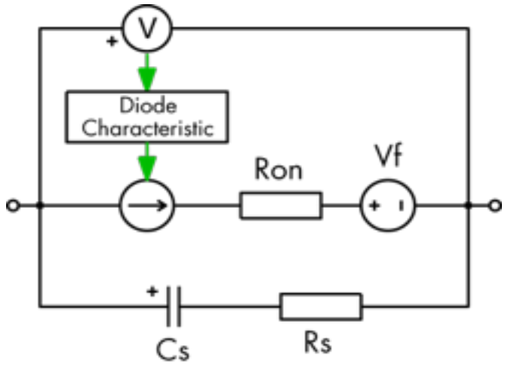
- Simplified switching transient (compared to physical model)
- Evaluation of EMI performance, voltage and current stress
- Can not be applied for power loss estimation and gate drive design
- Slow and poor convergence if applied to complex circuit model

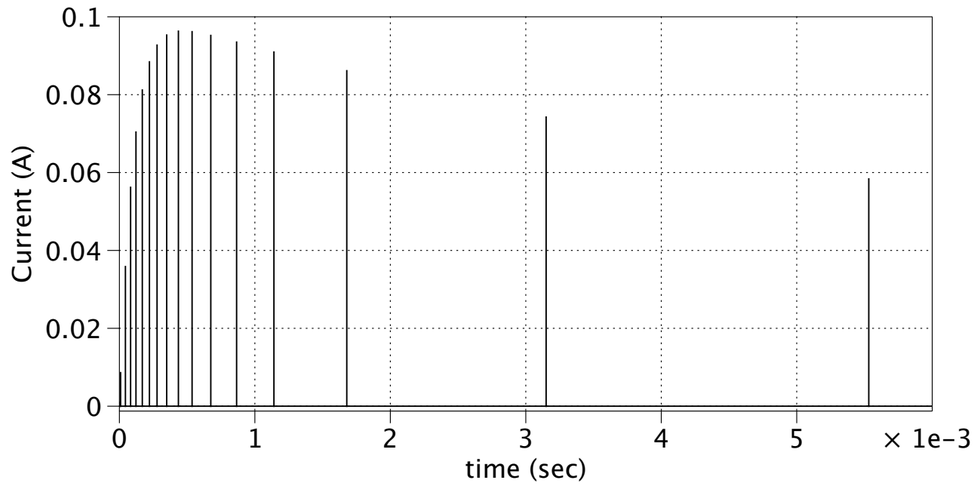


Model of Switching Devices - Resistor Model

Variable resistor model

- Small resistance in “on” state
- Large resistance in “off” state
- Implemented as voltage-controlled current source
- Switching transient has no physical meaning
- Additional snubber-circuit necessary for convergence
- Stiffness: Require extremely small time step

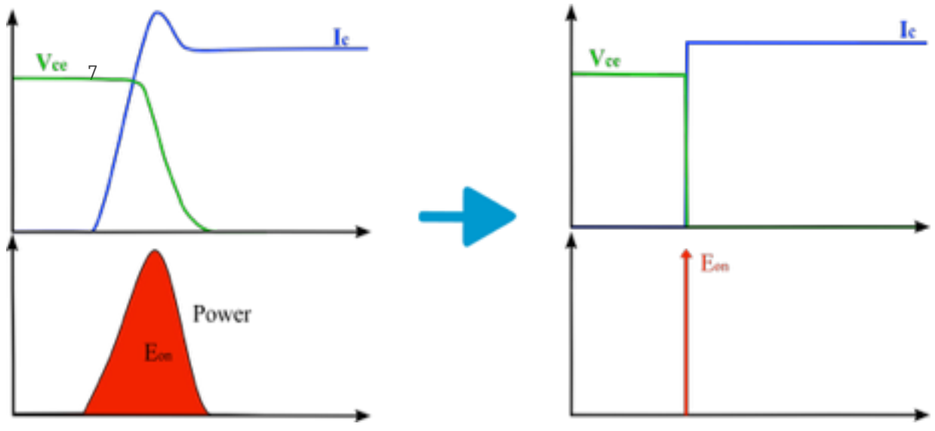


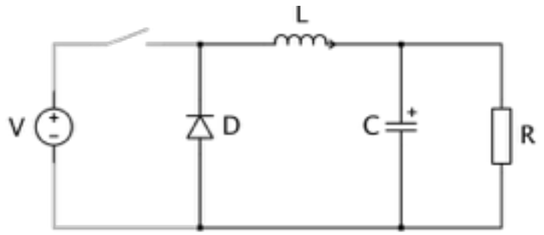


Model of Switching Devices - Ideal Switch

Ideal switch

- On state - short circuit
- Off state - open circuit
- Exchange state matrix after switch transition
- High speed, robust
- Optimal for HIL simulation





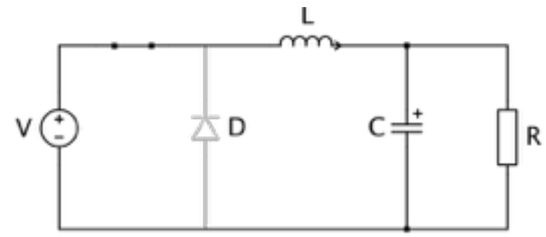
$$A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \quad D = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$x = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \quad y = \begin{bmatrix} v_D \\ i_D \end{bmatrix}$$

$$\dot{x} = Ax + Bu$$

$$y = Cx + Du$$

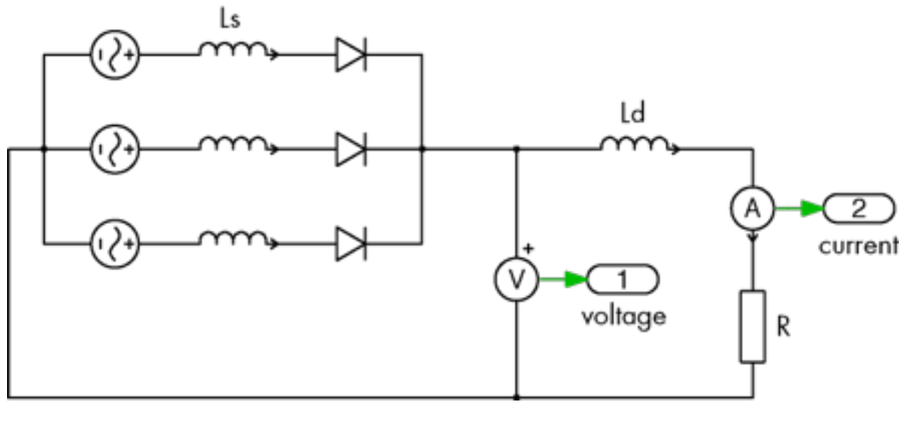


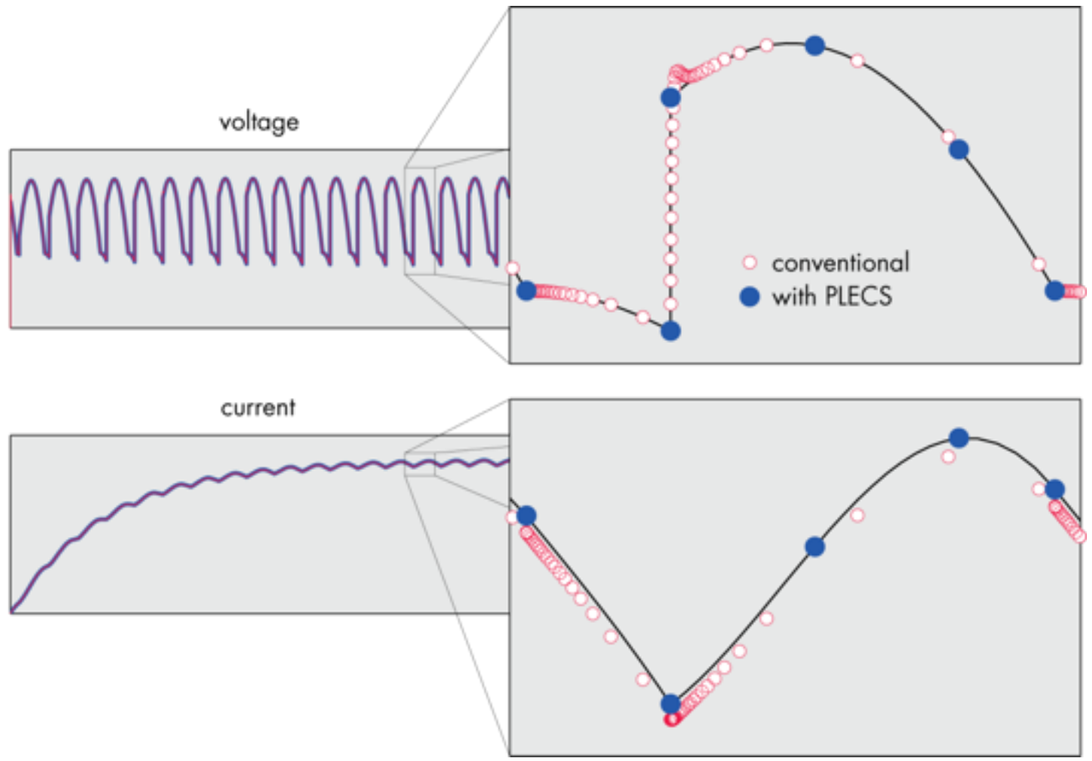
$$A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \quad D = \begin{bmatrix} -1 \\ 0 \end{bmatrix}$$

Comparison: Diode Rectifier

Simulation with variable resistance and ideal switches

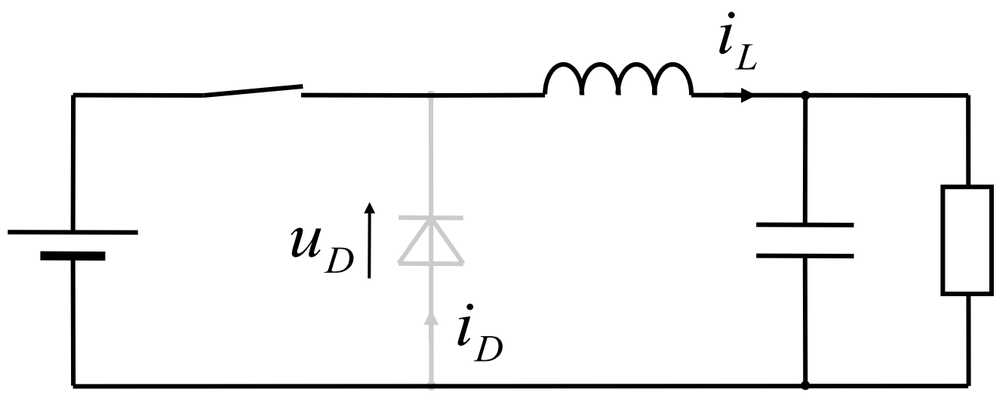


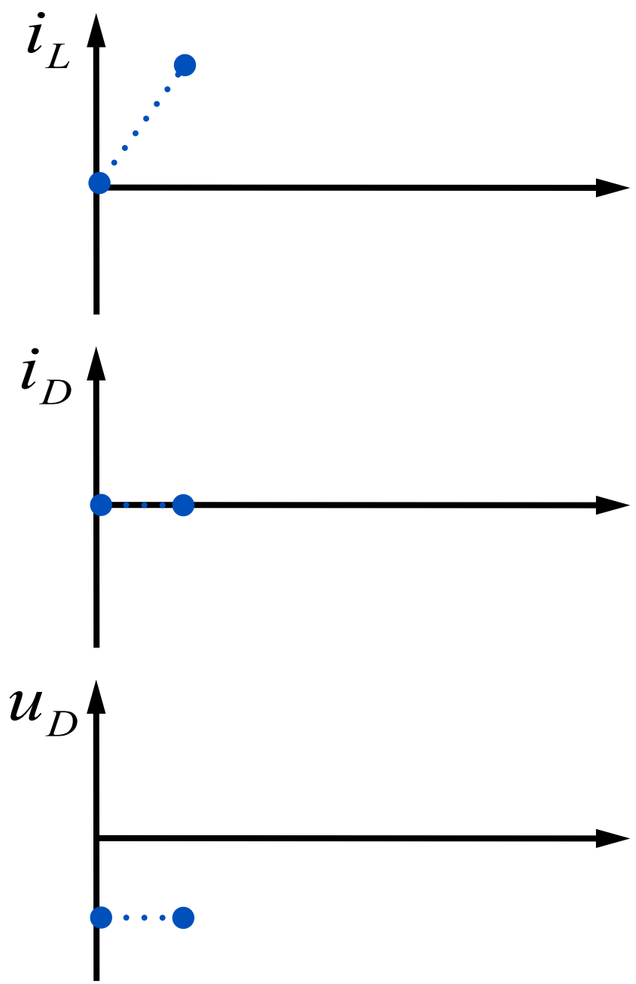


- Simulation steps:
  1160 → 153
- Computation time:
  0.6s → 0.08s

Ideal Switch: Buck Converter

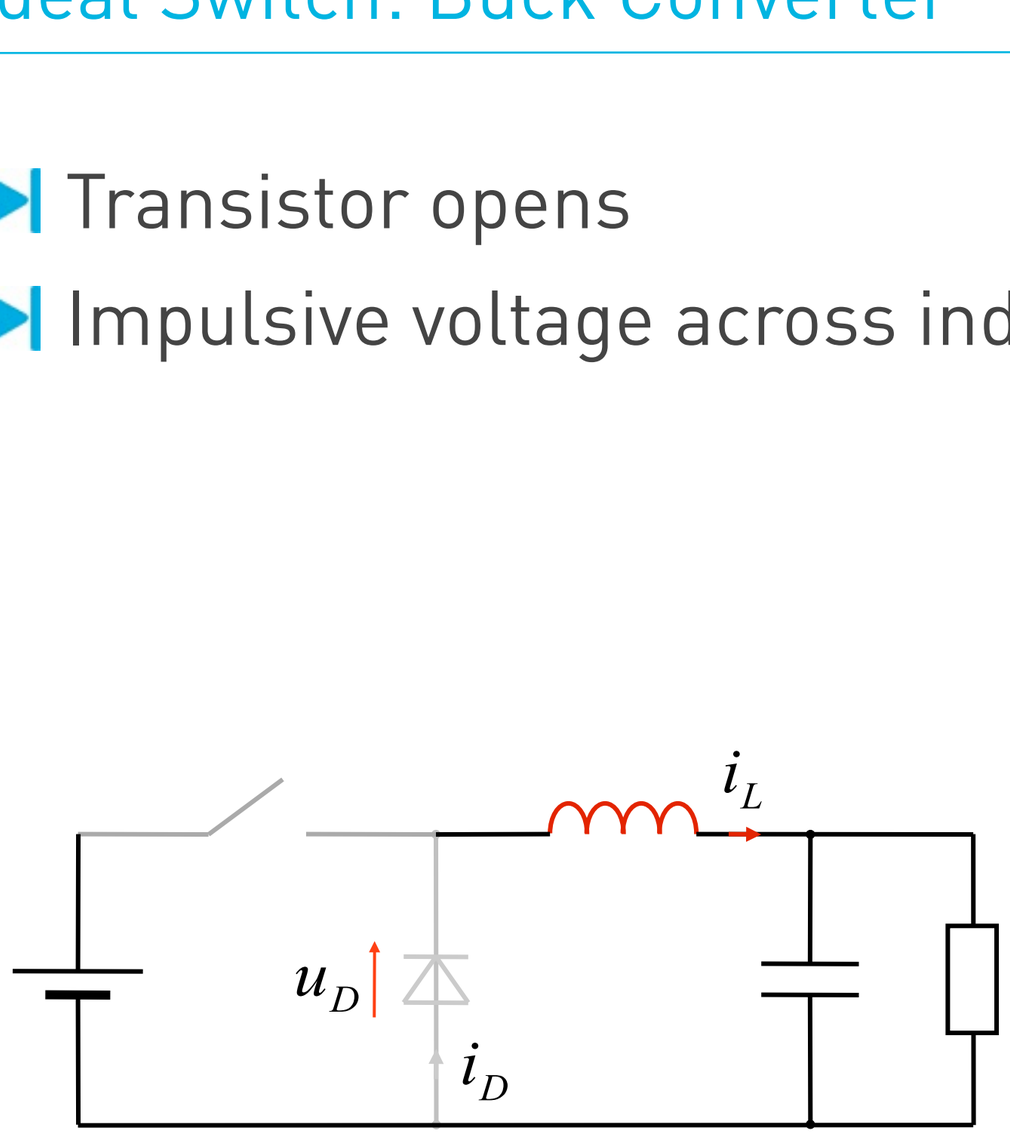
- Transistor conducts
- Diode blocks

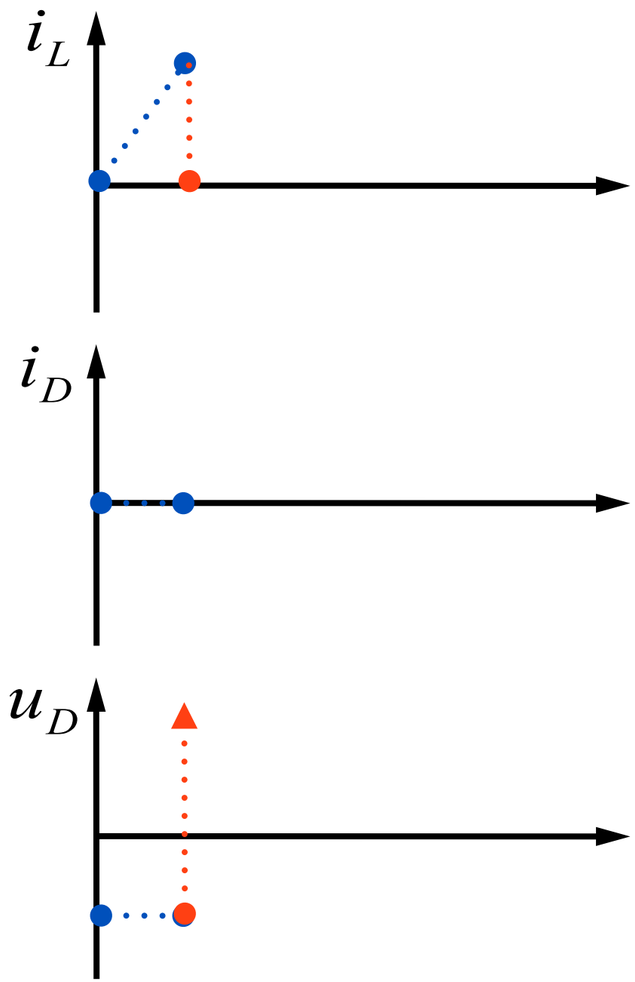




Ideal Switch: Buck Converter

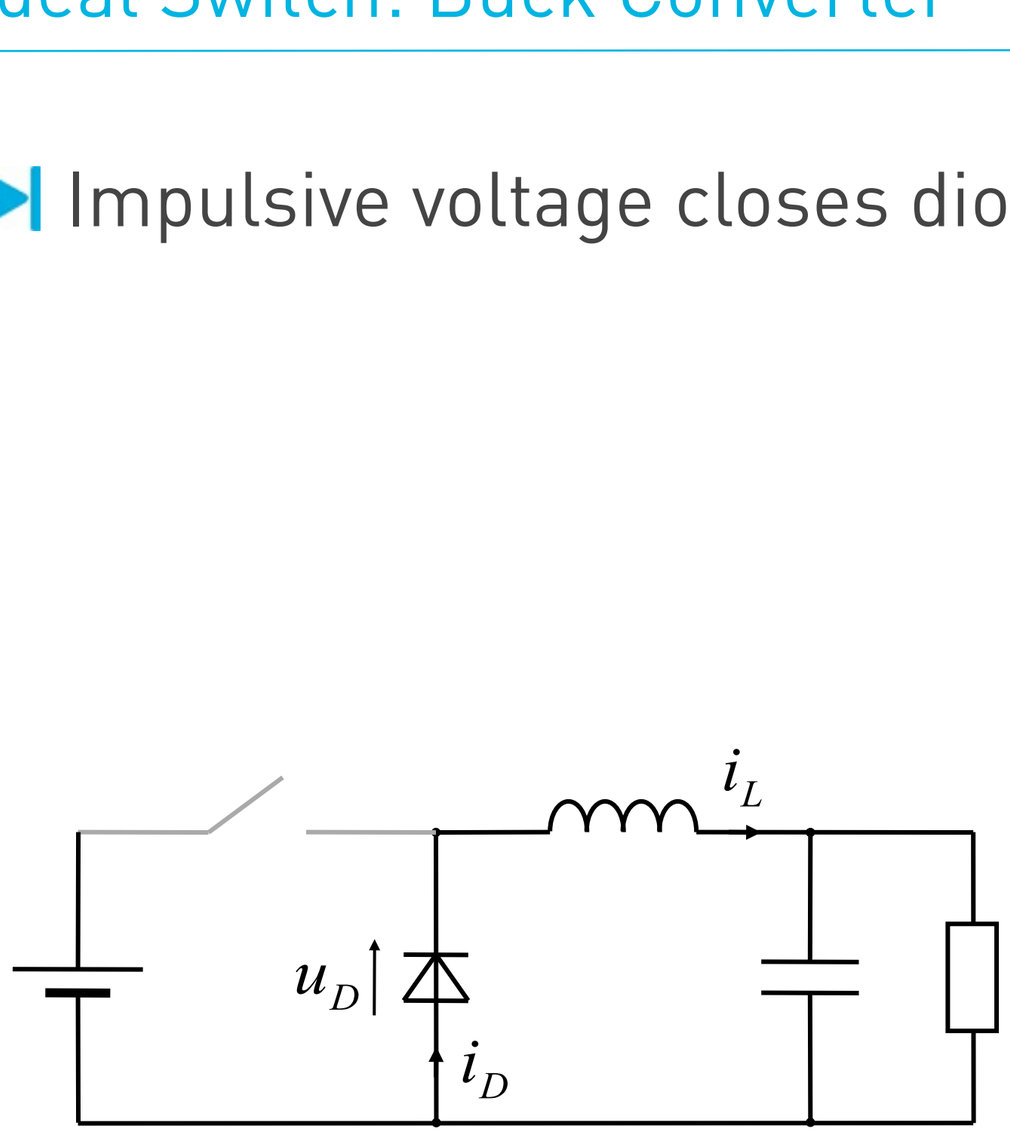
- Transistor opens
- Impulsive voltage across inductor

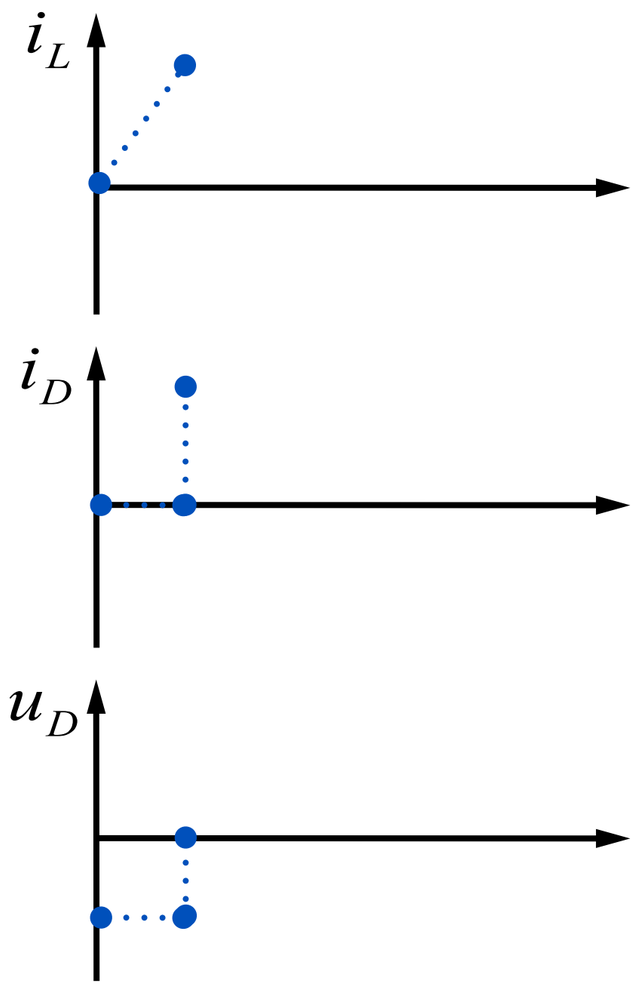




Ideal Switch: Buck Converter

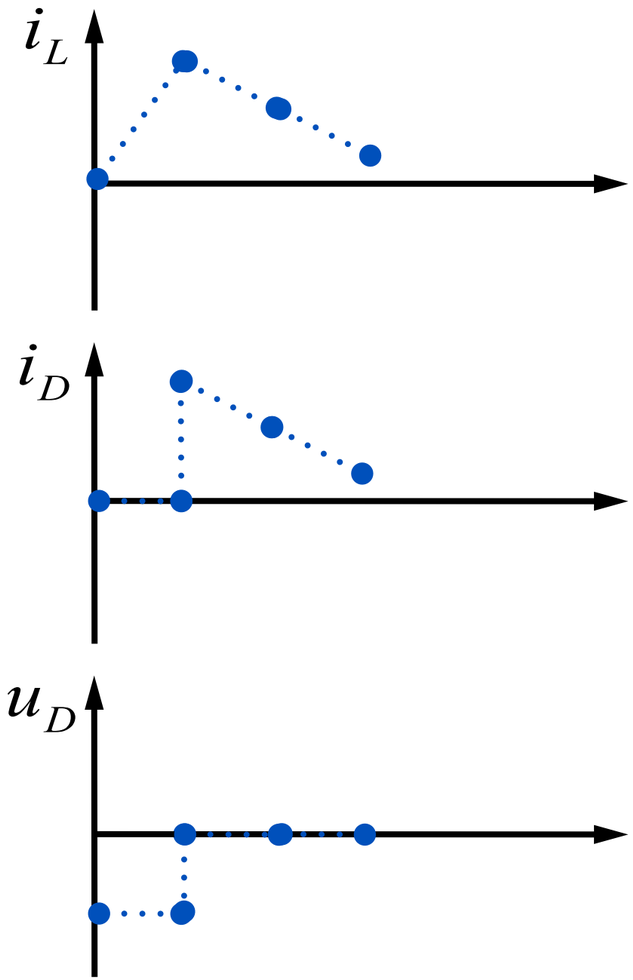
- Impulsive voltage closes diode

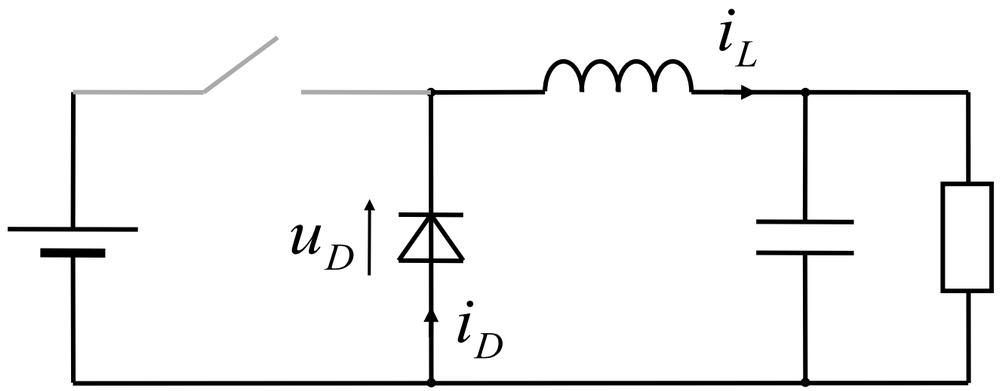




Ideal Switch: Buck Converter

- Transistor open
- Diode conducts

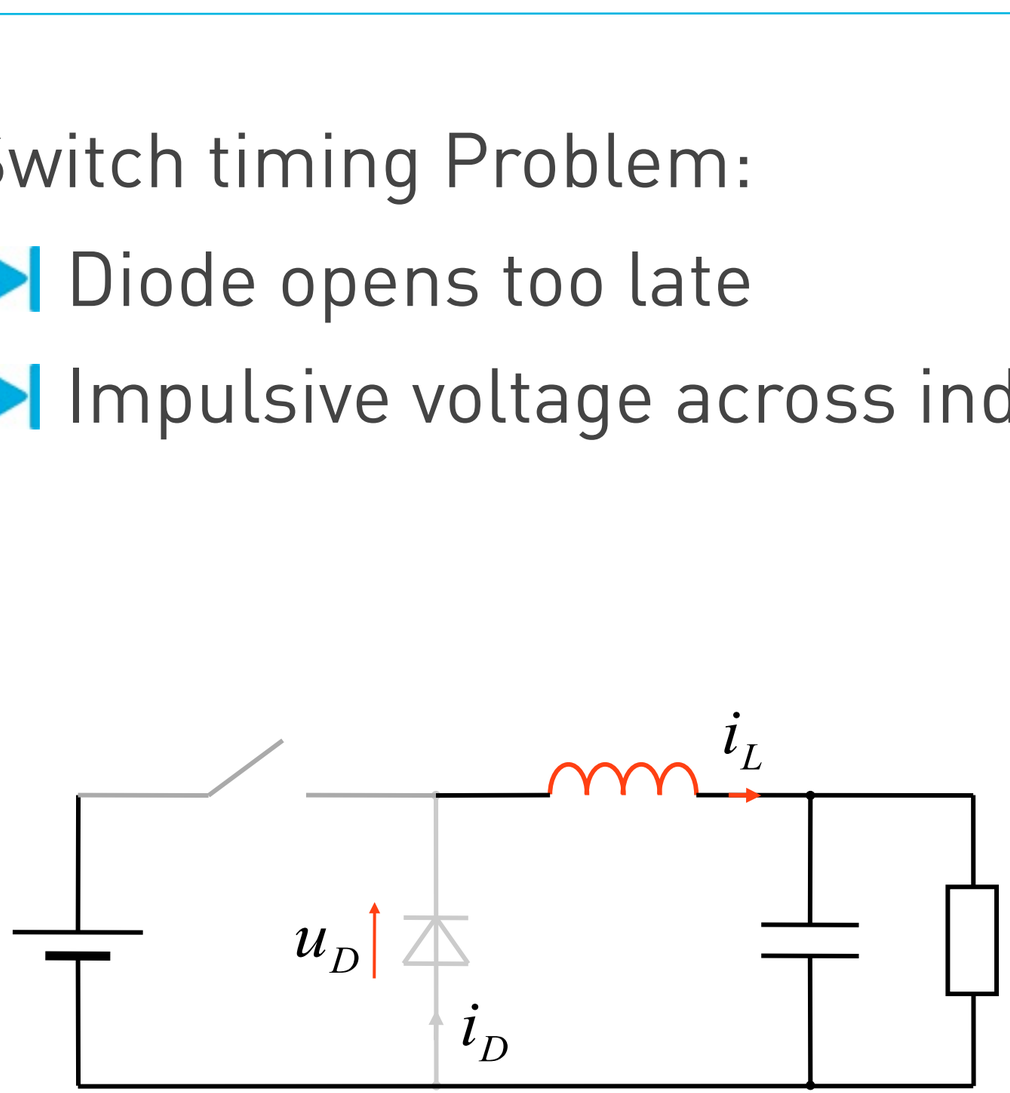


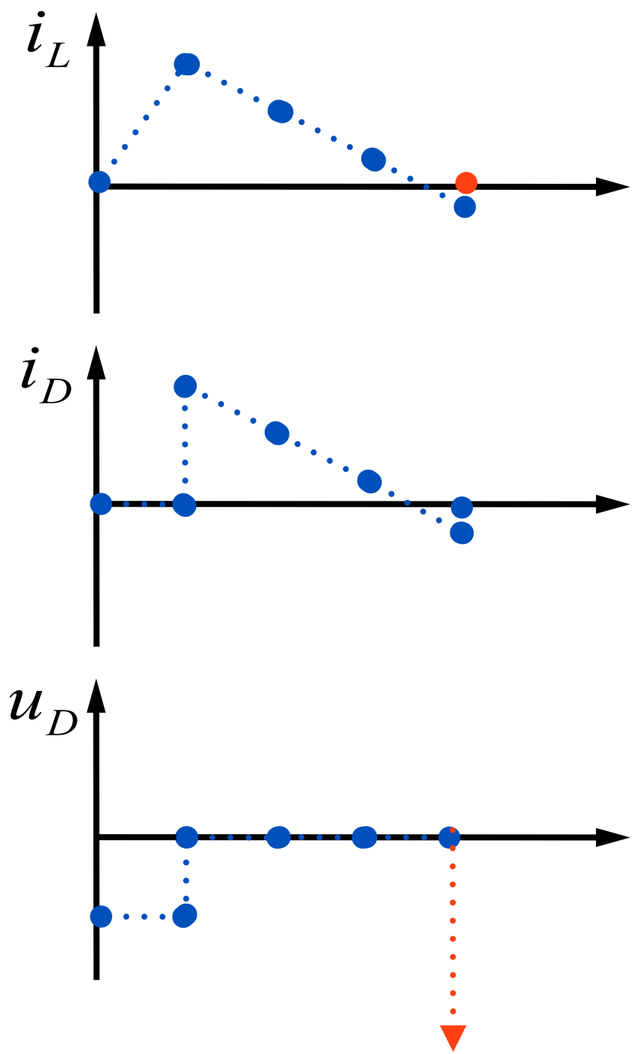


Ideal Switch: Buck Converter

Switch timing Problem:

- Diode opens too late
- Impulsive voltage across inductor

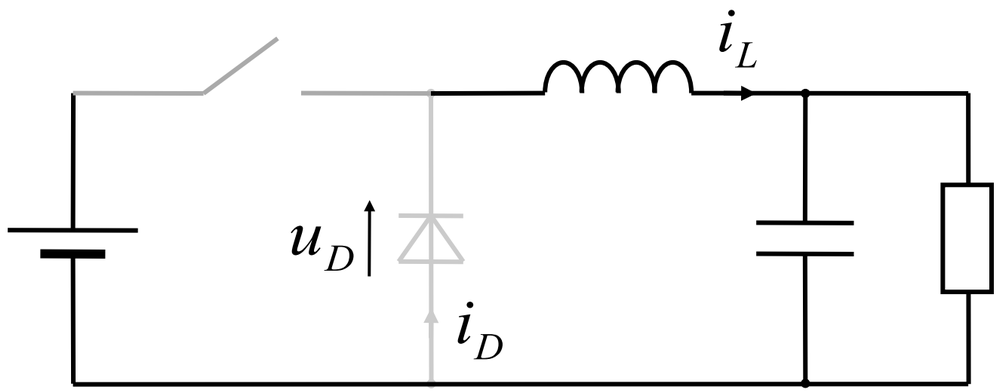


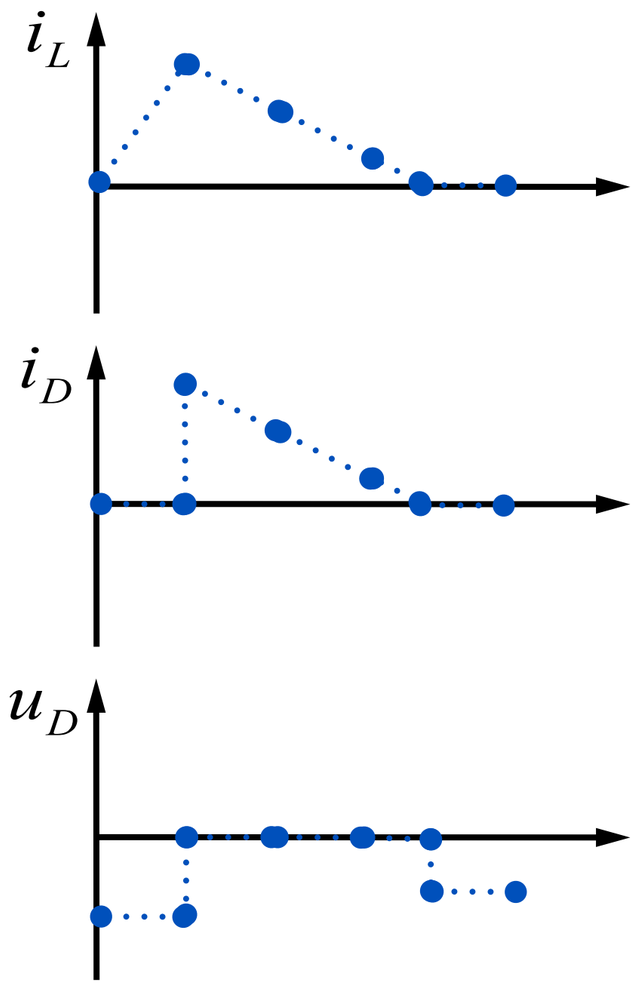


Ideal Switch: Buck Converter

Zero-crossing detection:

- Time step is reduced
- Diode opens at the zero-crossing

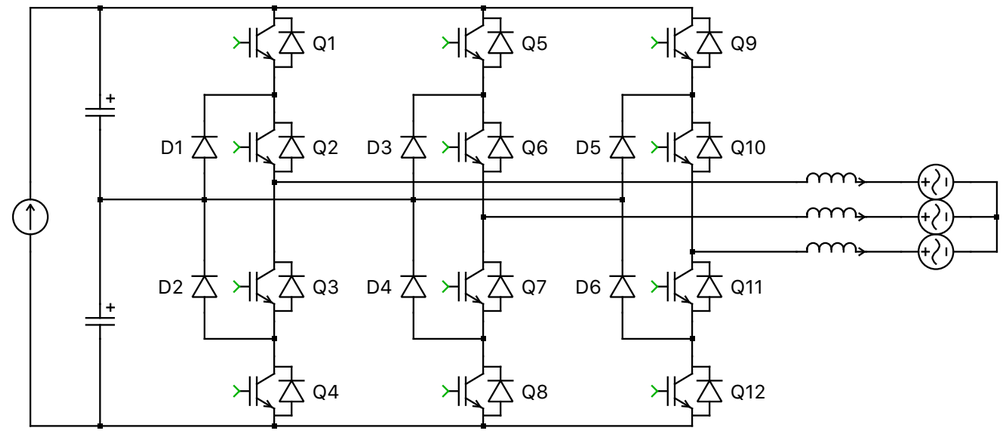




Modeling of Modules

Switches in complex topologies

- NPC: 18 switching devices
- Possible switching combinations 2^{18}
- Matrix dynamically generated in offline
- Matrix pre-generated in online



Exclude invalid combinations

- Short voltage source (e.g. Q1-Q4 on)
- Open inductive current (e.g. Q9-Q12 off)

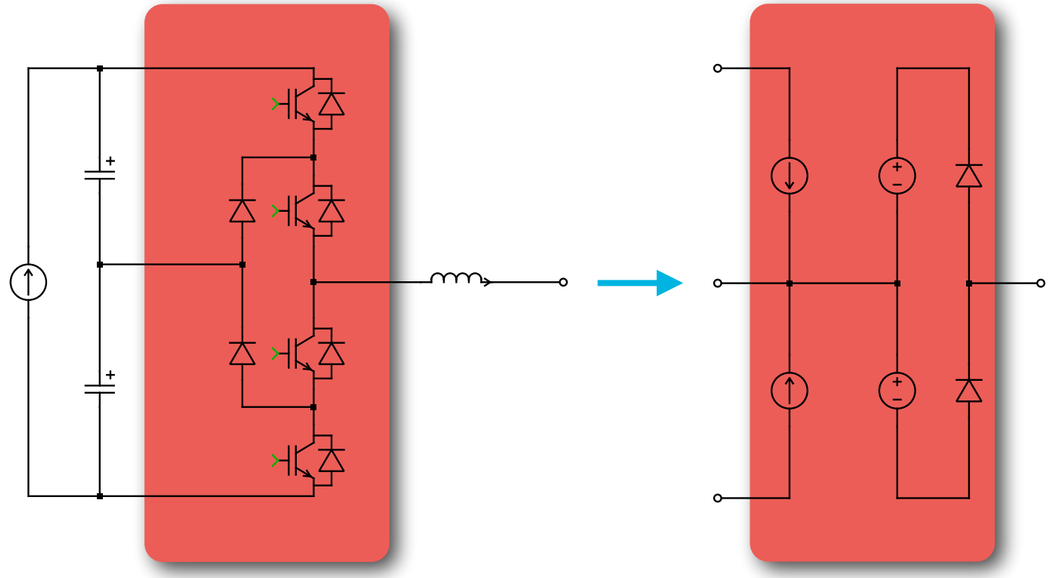
Further reduce matrixes

- Bring difficulty to code generation
- Time needed to choose new matrix

$$
\begin{array}{lcl}
\text{Switches} & \text{Q1 Q2 Q3 Q4 } \cdots \text{ D3 D4 D5 D6} & \\
1 & 0,\ 0,\ 1,\ 1,\ \ldots\ ,\ 0,\ 0,\ 0,\ 0 & \rightarrow A1\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} B1\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} C1\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} D1\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} \\
2 & 1,\ 1,\ 0,\ 0,\ \ldots\ ,\ 0,\ 0,\ 0,\ 0 & \rightarrow A2\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} B2\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} C2\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} D2\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} \\
3 & 0,\ 1,\ 1,\ 0,\ \ldots\ ,\ 0,\ 0,\ 0,\ 1 & \rightarrow A3\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} B3\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} C3\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} D3\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} \\
\vdots & \vdots & \vdots \\
n & 0,\ 1,\ 1,\ 0,\ \ldots\ ,\ 1,\ 0,\ 0,\ 0 & \rightarrow An\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} Bn\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} Cn\begin{bmatrix}\cdots\\ \cdots\end{bmatrix} Dn\begin{bmatrix}\cdots\\ \cdots\end{bmatrix}
\end{array}
$$

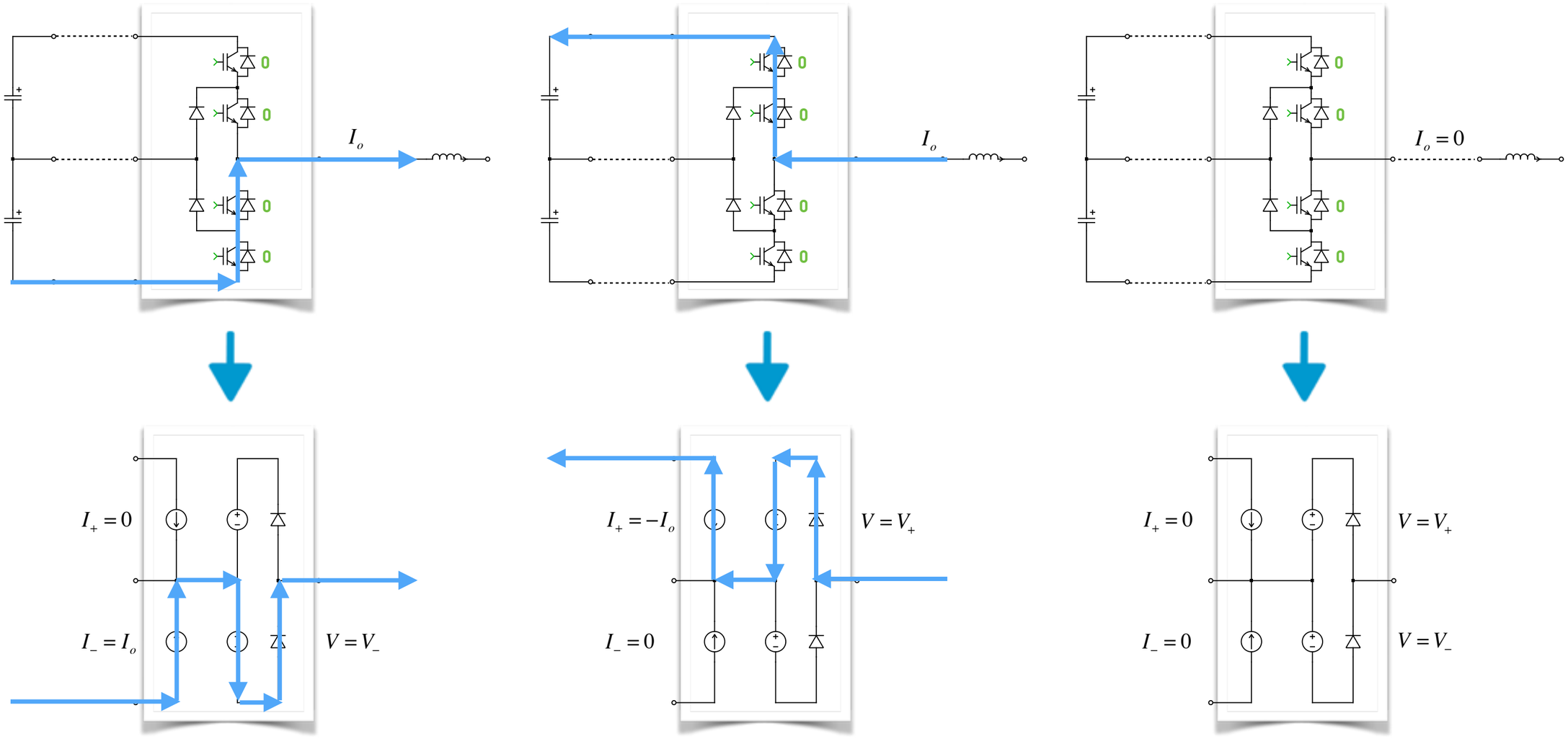
Modeling of Modules

- Equivalent modules
  - Voltage source on AC side
  - Current source on DC side
  - Same behavior as switched model
- Clamping diode
  - For free wheeling
  - 6 switches reduced to 2
- Difference compared to conventional source model
  - Taking into account blanking time
  - Account for inactive state
  - Simulating starting process (charing the capacitor)
  - Simulating fault condition (e.g. part of the devices loosing gate signal)



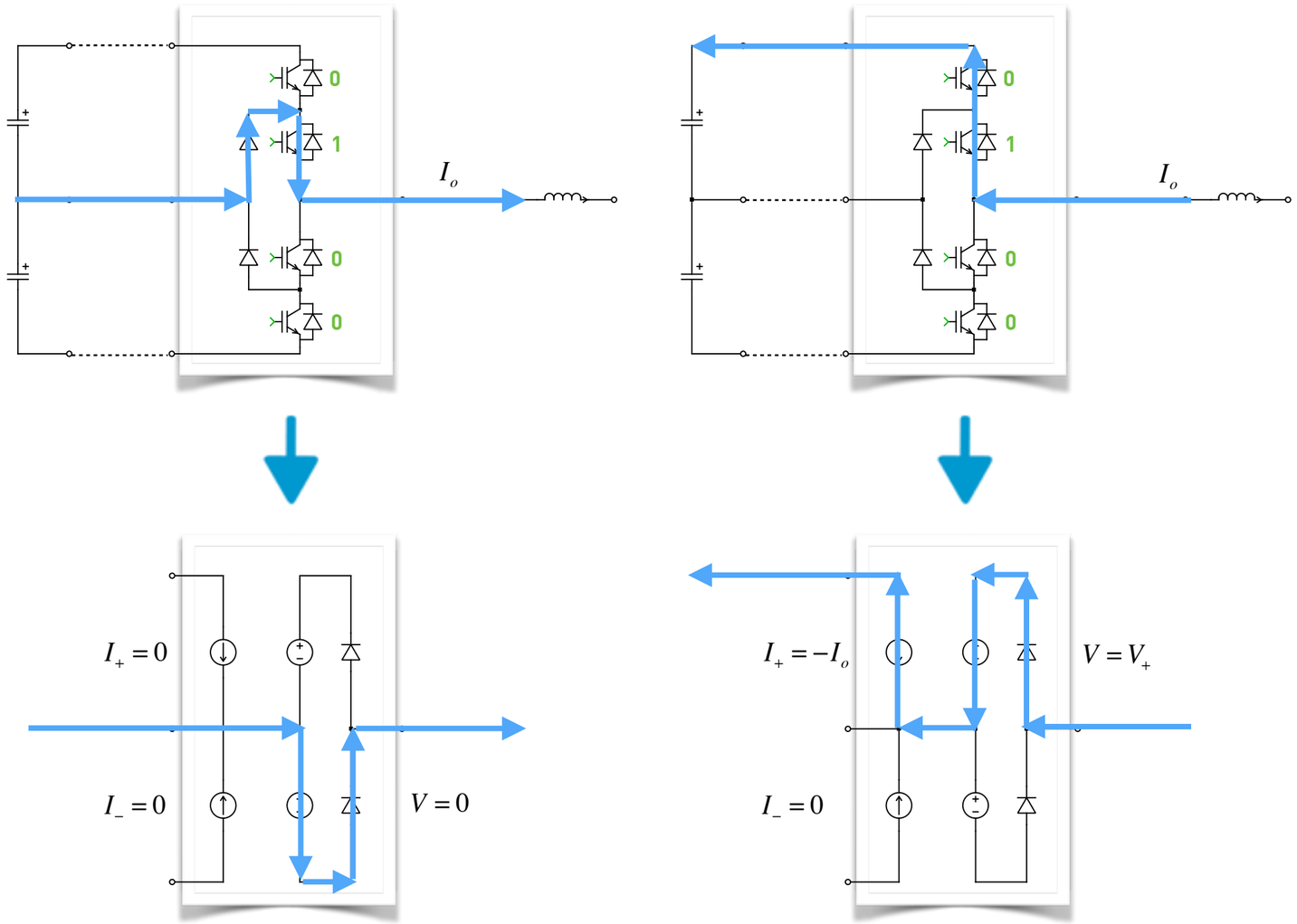
Modeling of Modules

Example: NPC bridge



Modeling of Modules

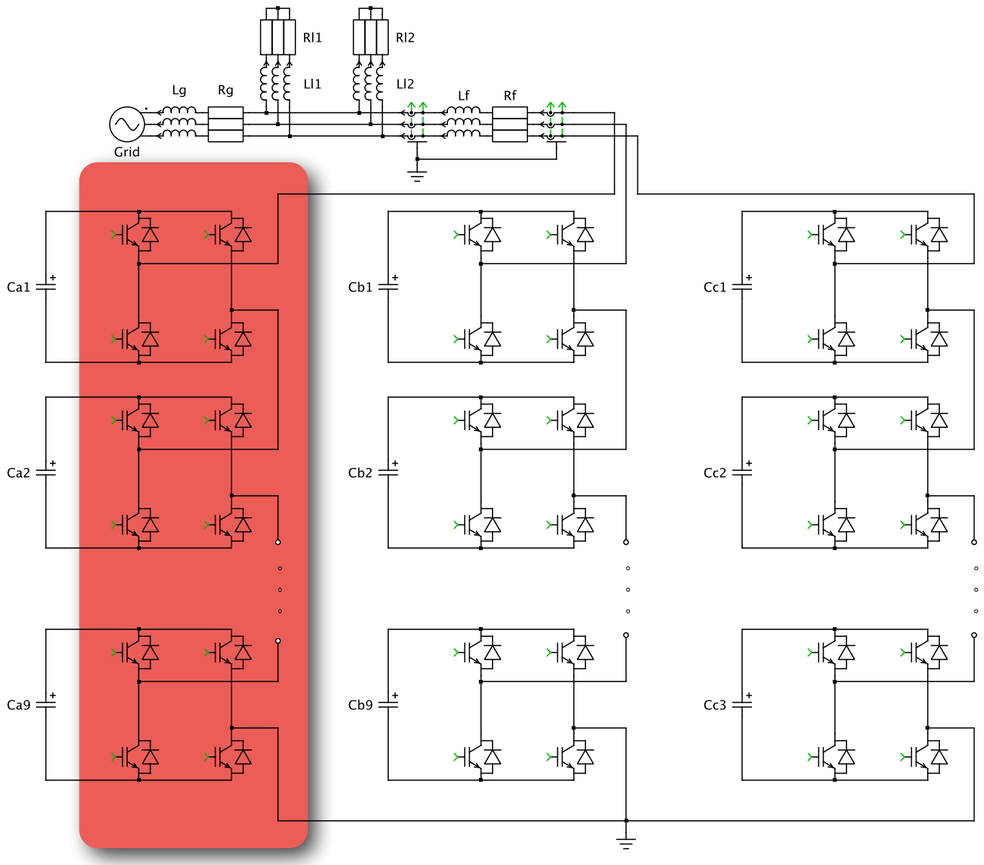
Example: NPC bridge

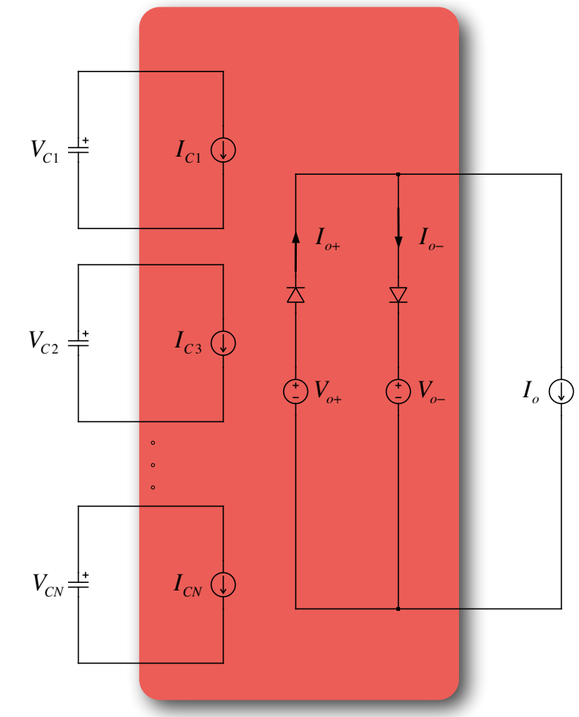


Modeling of Modules

Example: Cascaded H-bridges

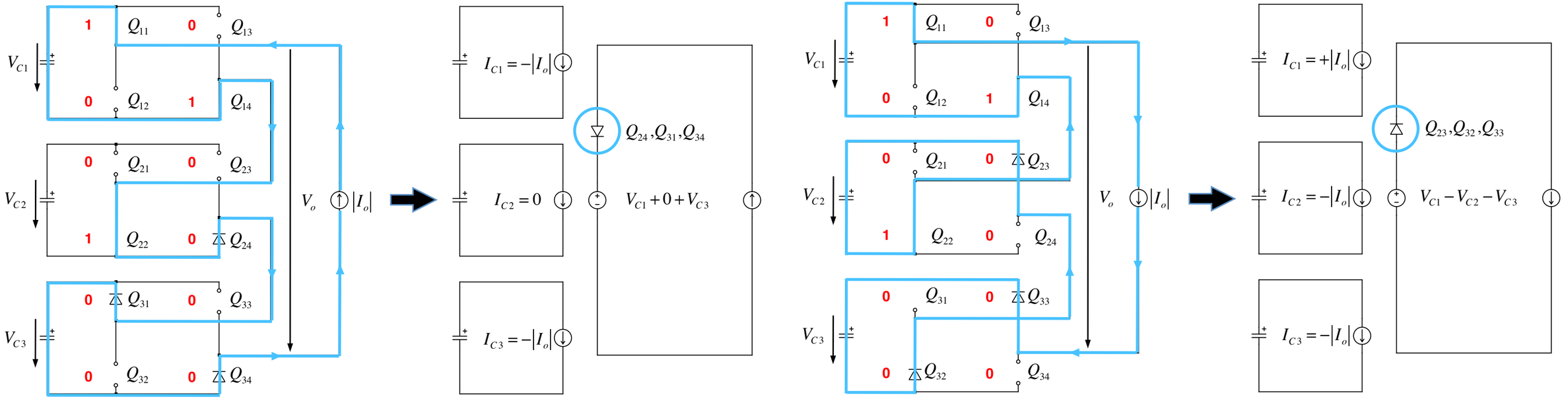
- The whole module (arbitrary number of series connection) only has two diodes
- Reduce model size effectively



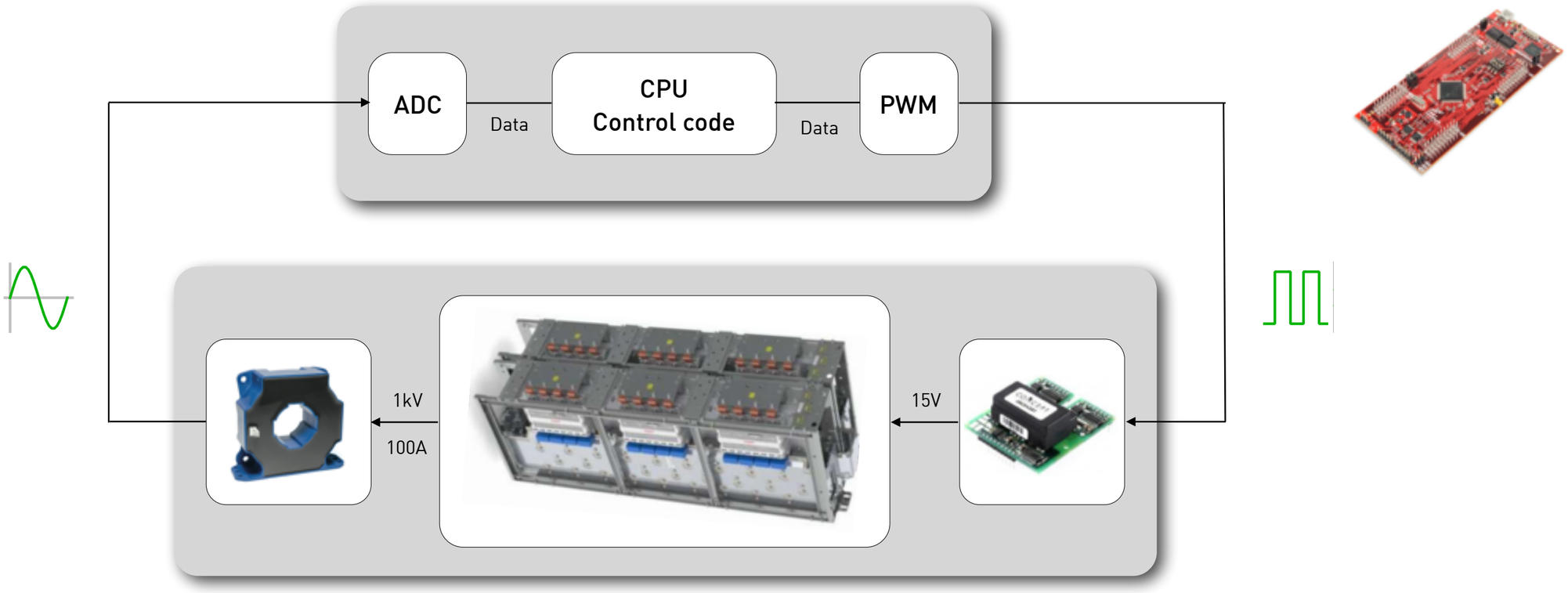


Modeling of Modules

Example: Cascaded H-bridges

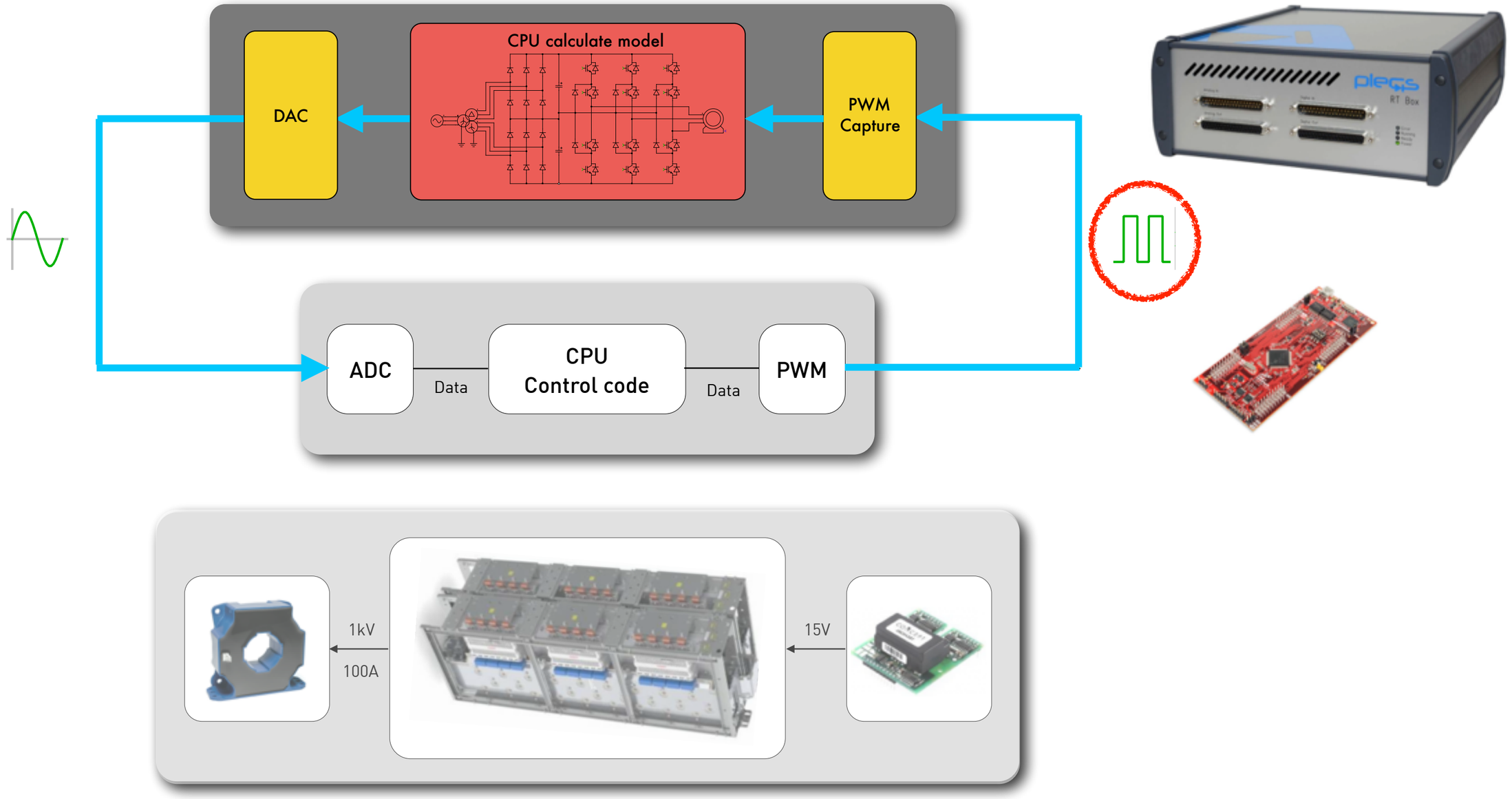


HIL Structure - 1



Include figures from Semikron, TI, LEM, Concept website

HIL Structure - 2



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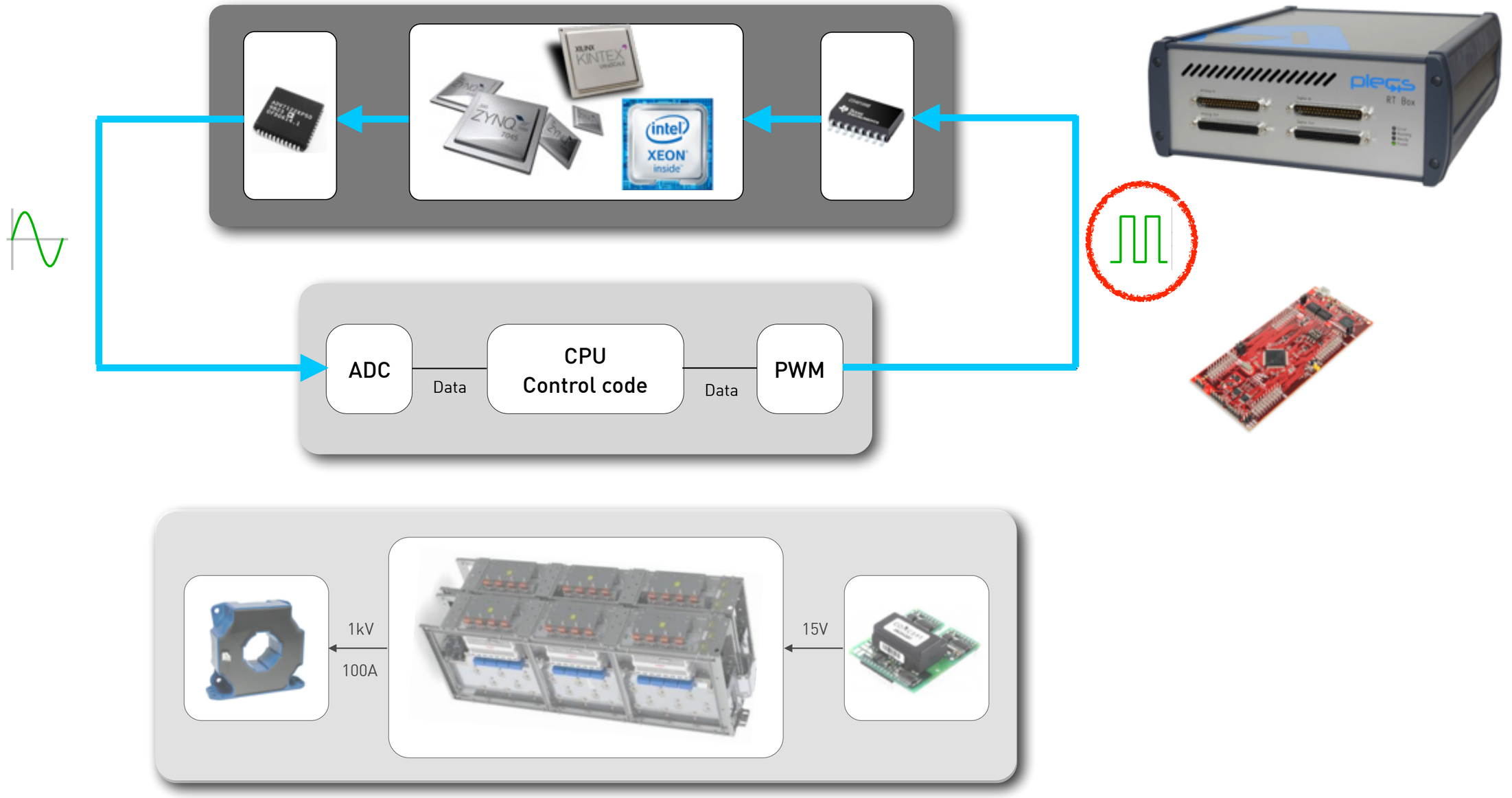
HIL Structure - 3



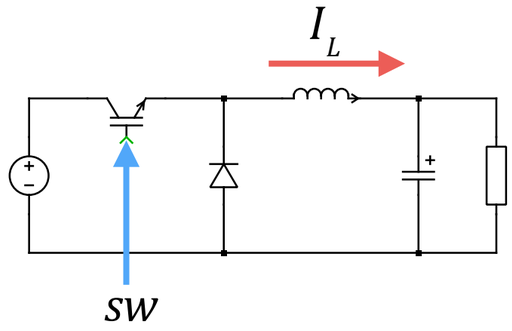
Include figures from Semikron, TI, LEM, Concept, Xilinx, Intel, Analog Devices website

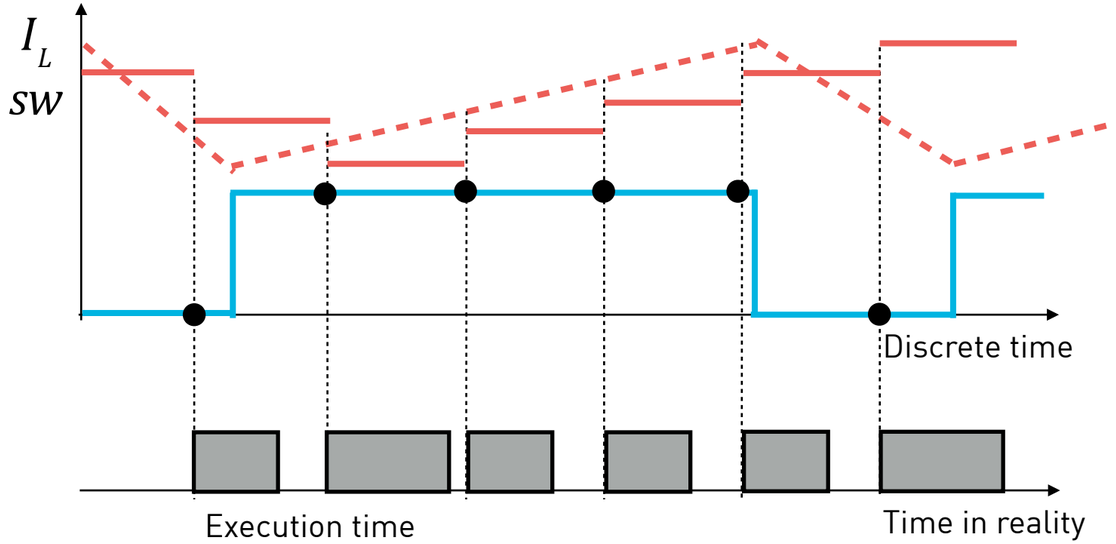
Offline and HIL Simulation in Common

- Both calculate models
  - In CPU or FPGA
  - Discretised in time domain
- No substantial difference
- How is a circuit model solved?

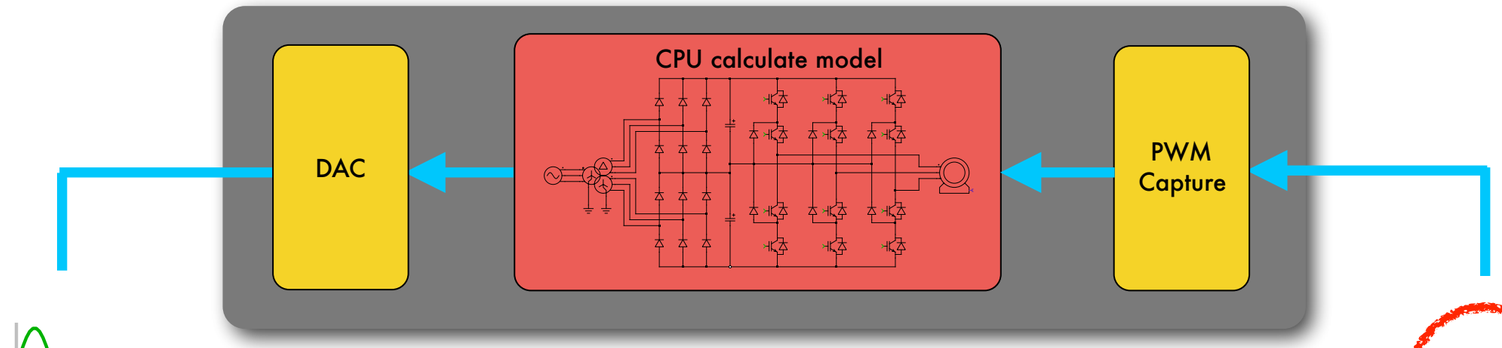
Challenge in HIL Simulations

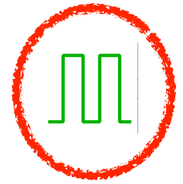
- Discretisation step size
- Small step size desired
  - Guarantee accuracy
  - Limited by computation power
  - Limited by IO latency
- T_{disc} larger than $T_{execute}$
  - Depends on model complexity
  - Resolution of PWM gate signal
  - What if T_{disc} smaller than $T_{sw}/10$ can not be fullfilled ???

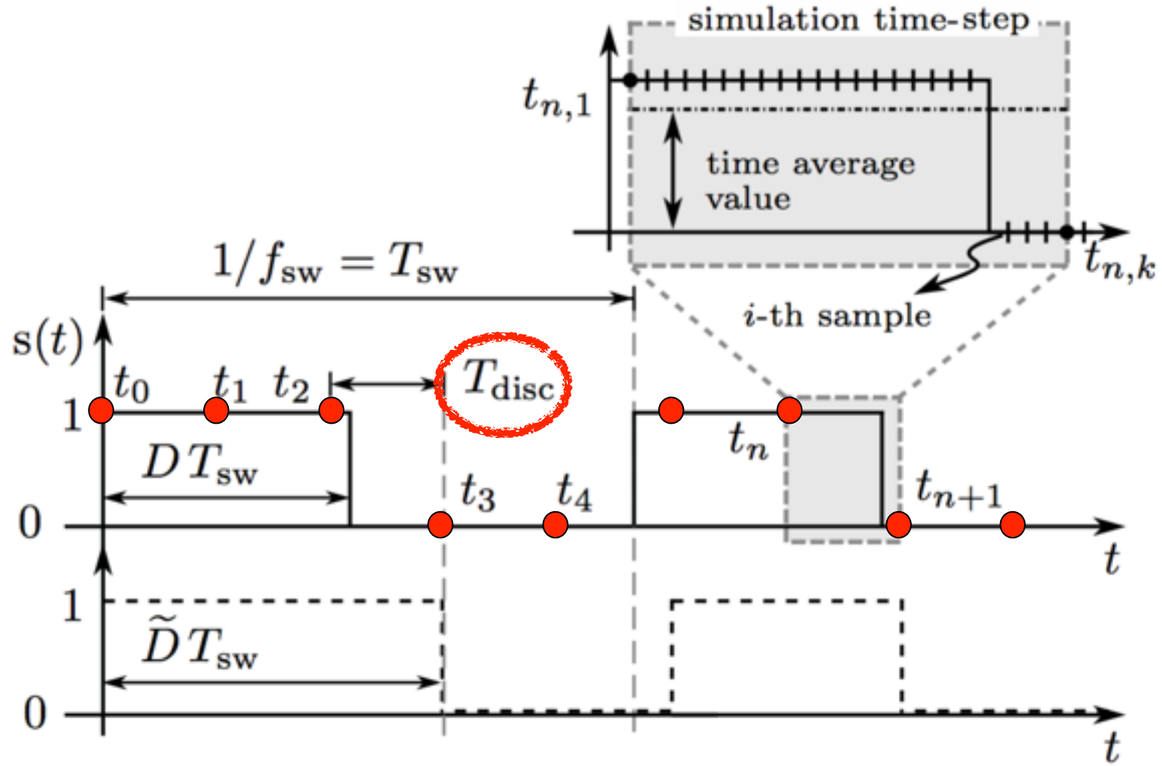




PWM Sampling - 1



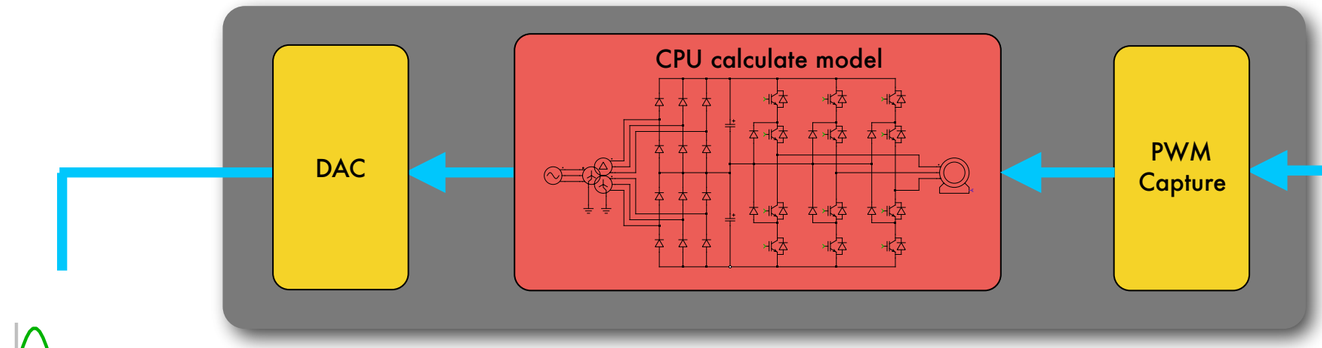


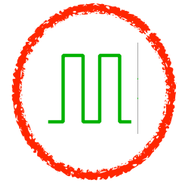


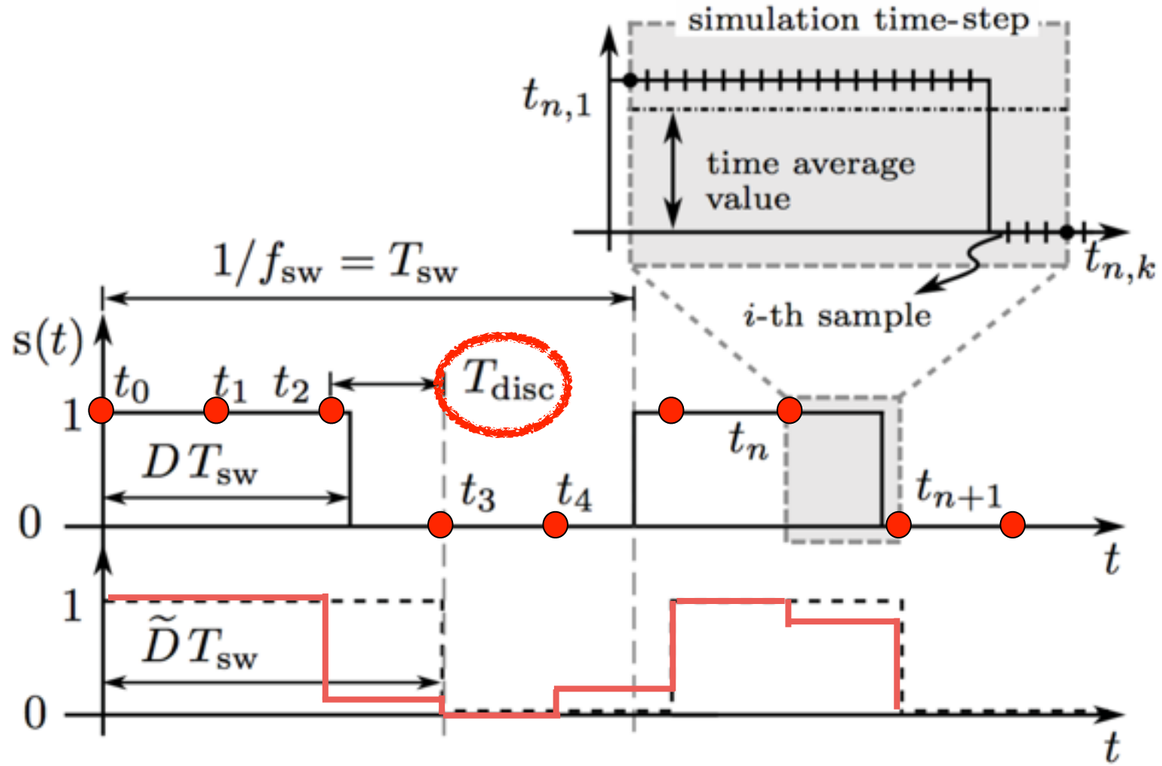
Sample PWM signal with
high resolution clock (e.g. 100MHz),
averaged signal from
the previous Tdisc
is provided to the model

Include figures from Semikron, TI, LEM, Concept website

PWM Sampling - 2







Sample PWM signal with
high resolution clock (e.g. 100MHz),
averaged signal from
the previous Tdisc
is provided to the model

Information of the PWM
signal accurately reflected

Include figures from Semikron, TI, LEM, Concept website

Model with Sub-cycle Averaged Switching Signals

Buck module

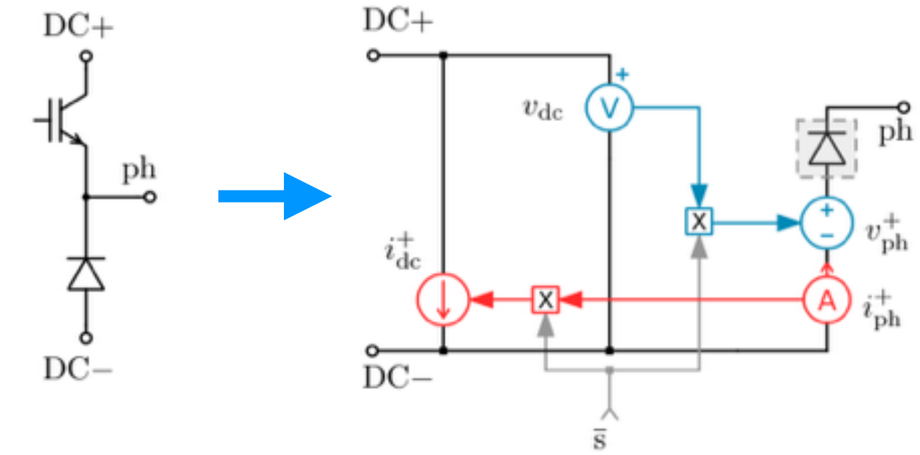
Sub-cycle averaged switching signal

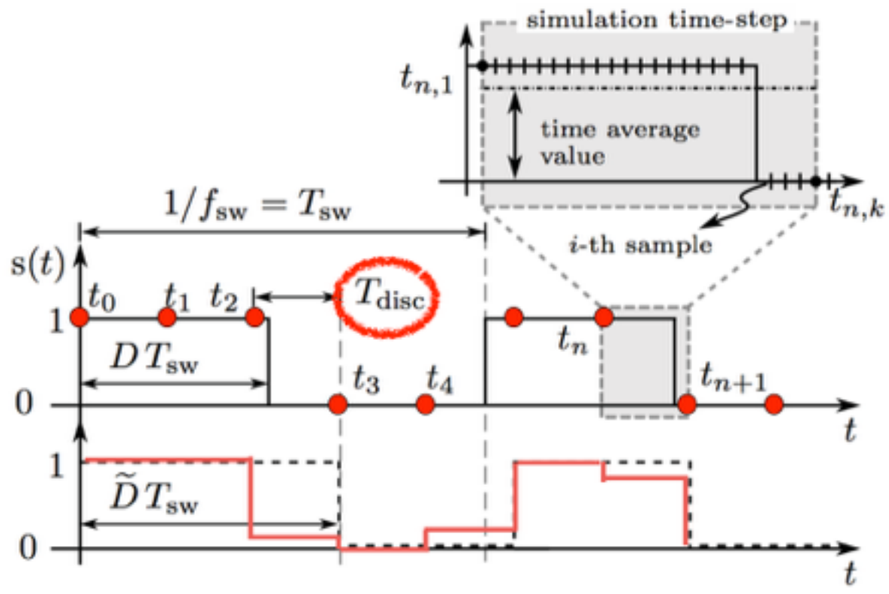
$$\overline{s}\big((n+1)\,T_{\text{disc}}\big) = \frac{1}{k}\cdot\sum_{i=1}^{k} \mathrm{s}\big((n+\tfrac{i}{k})\,T_{\text{disc}}\big)$$

Controlled sources

$$v_{ph}^{+} = \overline{s}\cdot v_{dc} \qquad i_{dc}^{+} = \overline{s}\cdot i_{ph}^{+}$$

Diode accounts for discontinuous current mode and inactive state





Model with Sub-cycle Averaged Switching Signals

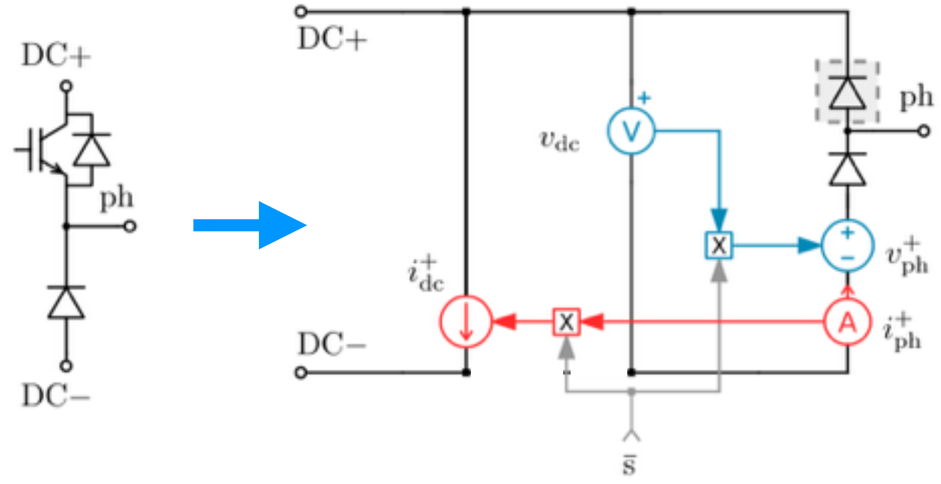
- IGBT with free wheeling diode
  - Sub-cycle averaged switching signal

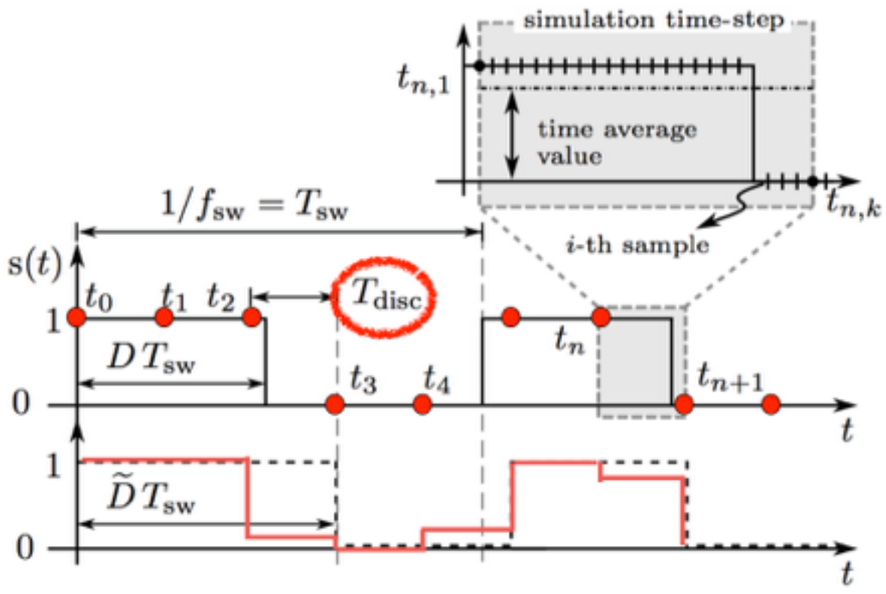
$$\overline{s}\big((n+1)\,T_{\text{disc}}\big) = \frac{1}{k}\cdot\sum_{i=1}^{k} \mathrm{s}\big((n+\tfrac{i}{k})\,T_{\text{disc}}\big)$$

  - Controlled sources

$$v_{ph}^{+} = \overline{s}\cdot v_{dc} \qquad i_{dc}^{+} = \overline{s}\cdot i_{ph}^{+}$$

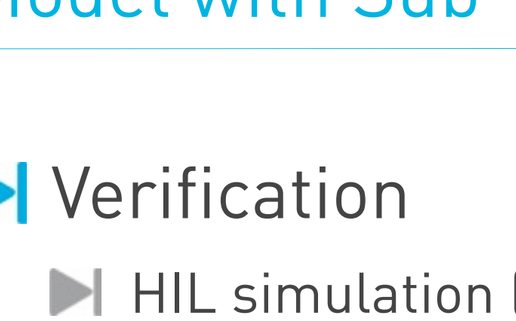
- Diodes account for discontinuous current mode and inactive state



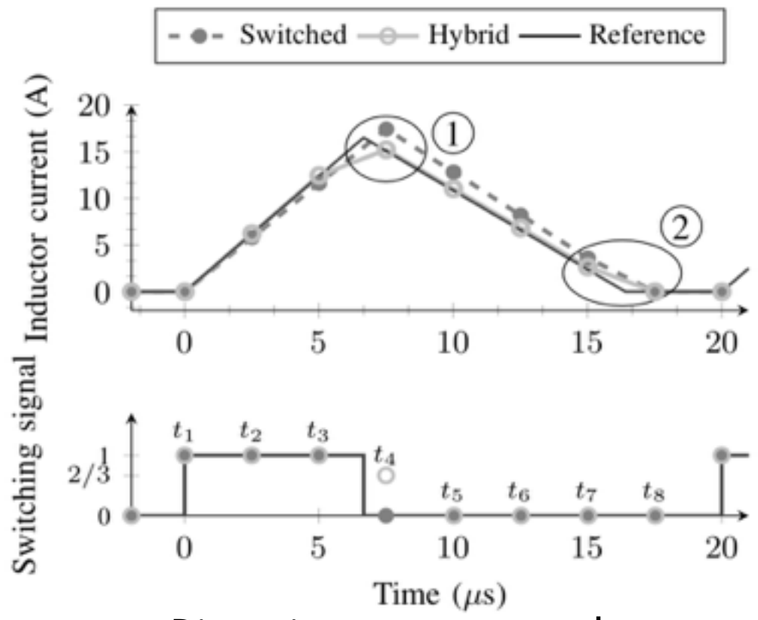


Model with Sub-cycle Averaged Switching Signals

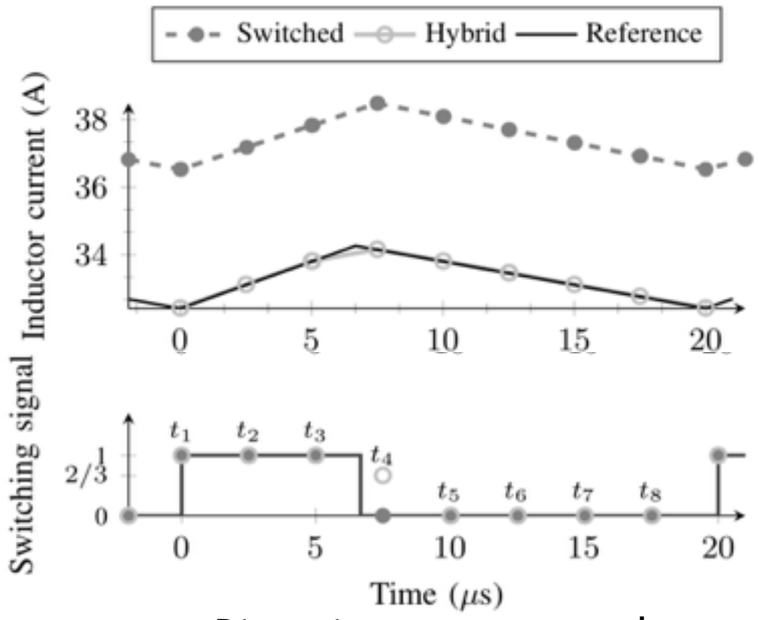
- Verification
  - HIL simulation (fixed step) compared with offline simulation (variable step)
  - Without sub-cycle average result deviated much from reference
  - With sub-cycle average matches reference well



Buck converter with Vdc = 500V
and duty cycle =1/3,



Discontinuous current mode
with L = 120uH, R = 30



Discontinuous current mode
with L = 1200uH, R = 5

Model with Sub-cycle Averaged Switching Signals

IGBT with free wheeling diode

- Sub-cycle averaged switching signal

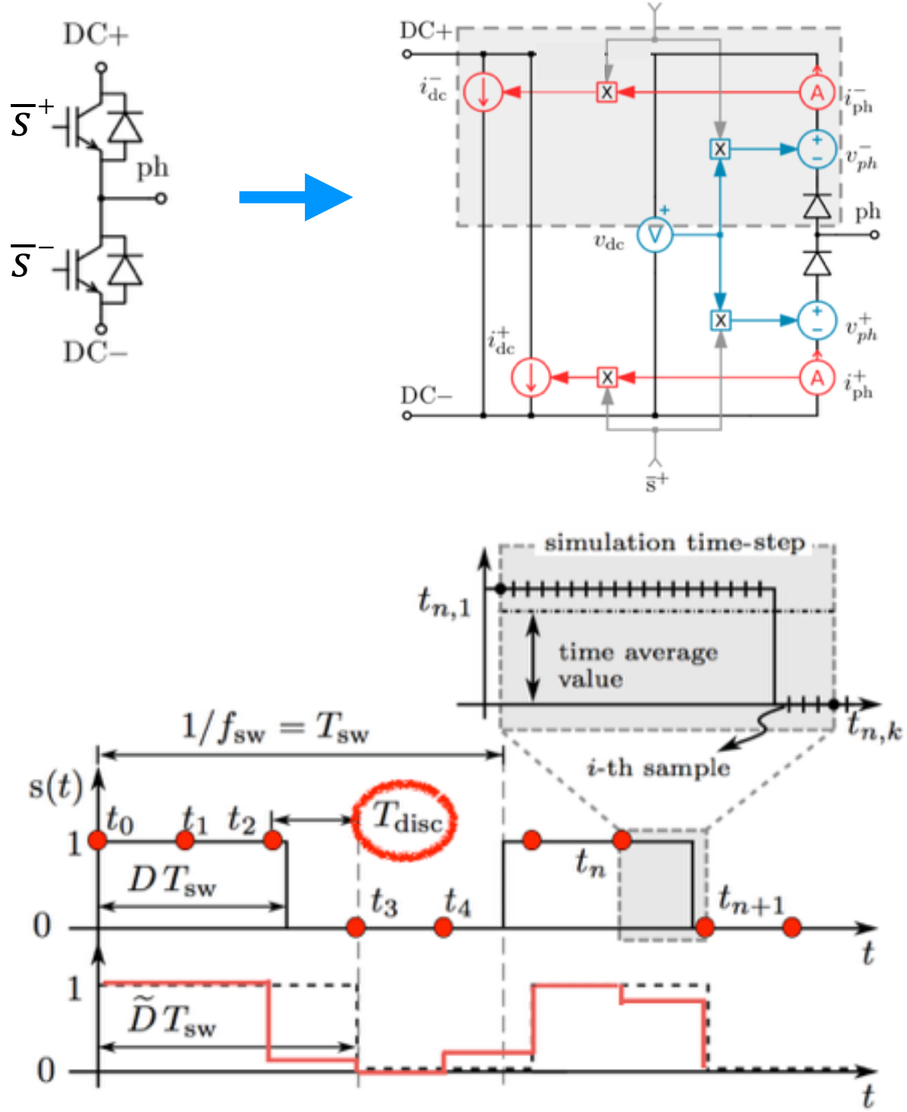
$$\overline{s}\left((n+1)\,T_{\text{disc}}\right) = \frac{1}{k}\cdot\sum_{i=1}^{k} \mathrm{s}\left((n+\tfrac{i}{k})\,T_{\text{disc}}\right)$$

- Controlled sources

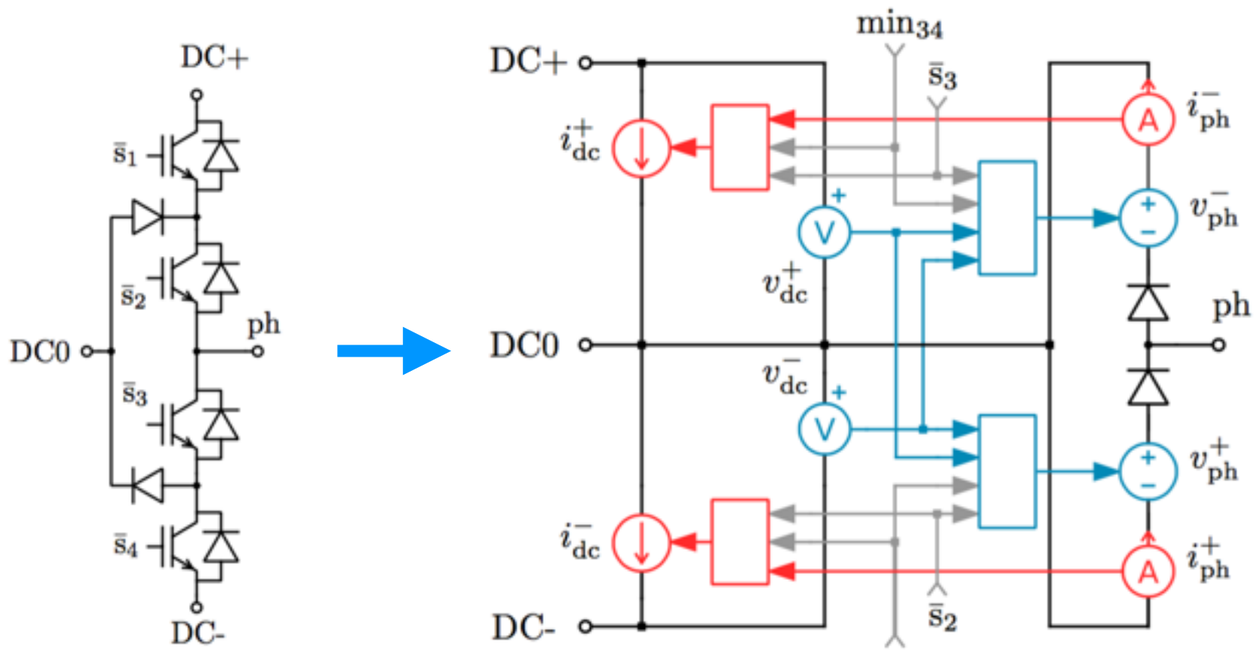
$$v_{ph}^{+} = \overline{s}^{+}\cdot v_{dc} \qquad i_{dc}^{+} = \overline{s}^{+}\cdot i_{ph}^{+}$$

$$v_{ph}^{-} = (\overline{s}^{-}-1)\cdot v_{dc} \qquad i_{dc}^{-} = (\overline{s}^{-}-1)\cdot i_{ph}^{-}$$

- Diodes account for discontinuous current mode and inactive state

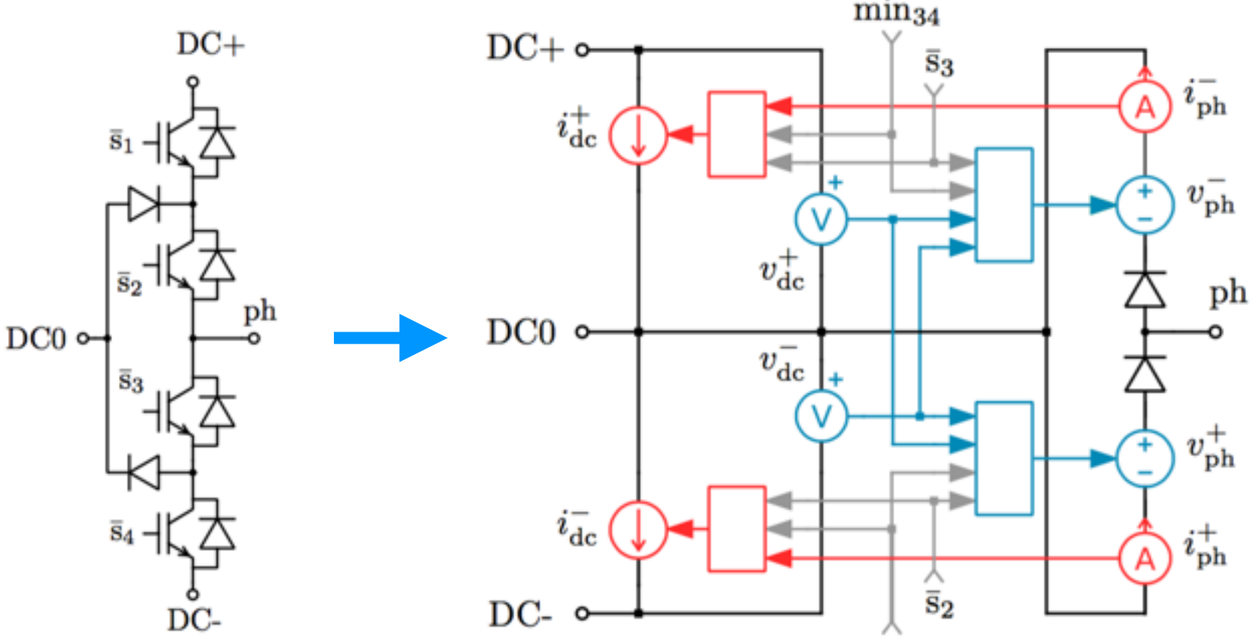


Model with Sub-cycle Averaged Switching Signals (NPC)



$$v_{\mathrm{ph}}^{+} = v_{\mathrm{dc}}^{+} \cdot \min_{12} - v_{\mathrm{dc}}^{-} \cdot (1 - \bar{s}_2)$$
$$v_{\mathrm{ph}}^{-} = v_{\mathrm{dc}}^{-} \cdot \min_{34} - v_{\mathrm{dc}}^{+} \cdot (1 - \bar{s}_3)$$
$$i_{\mathrm{dc}}^{+} = i_{\mathrm{ph}}^{+} \cdot \min_{12} - i_{\mathrm{ph}}^{-} \cdot (1 - \bar{s}_3)$$
$$i_{\mathrm{dc}}^{-} = i_{\mathrm{ph}}^{-} \cdot \min_{34} - i_{\mathrm{ph}}^{+} \cdot (1 - \bar{s}_2)$$

Model with Sub-cycle Averaged Switching Signals (NPC)

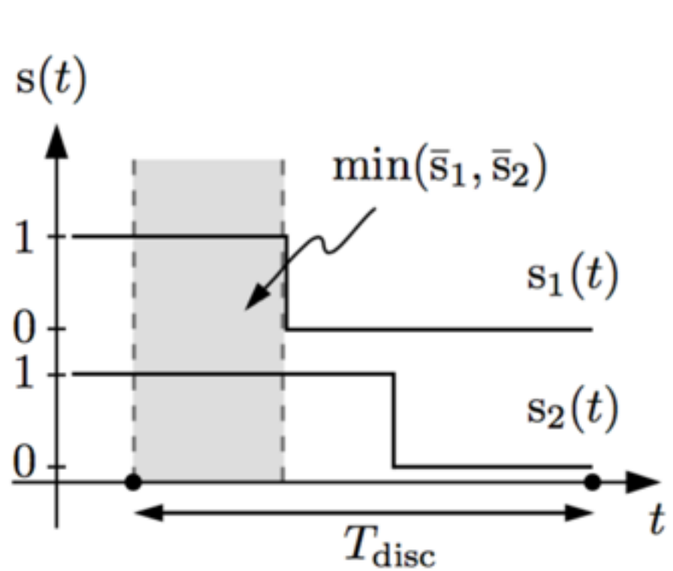


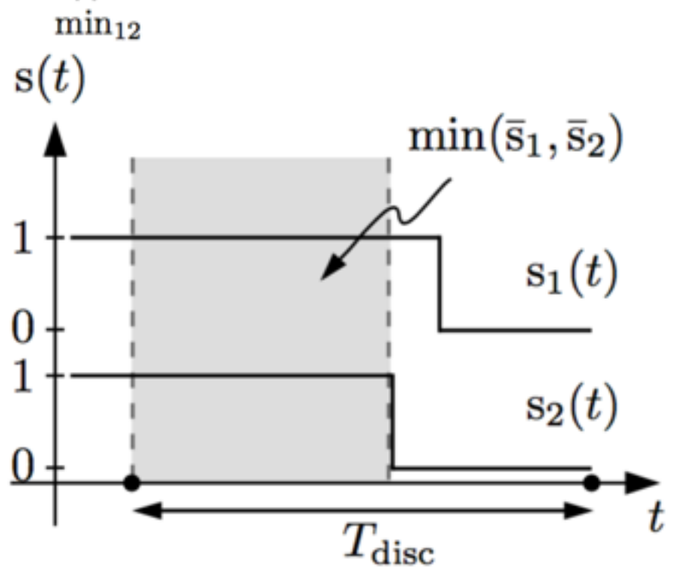
$$v_{ph}^+ = v_{dc}^+ \cdot \min_{12} - v_{dc}^- \cdot (1 - \bar{s}_2)$$

$$v_{ph}^- = v_{dc}^- \cdot \min_{34} - v_{dc}^+ \cdot (1 - \bar{s}_3)$$

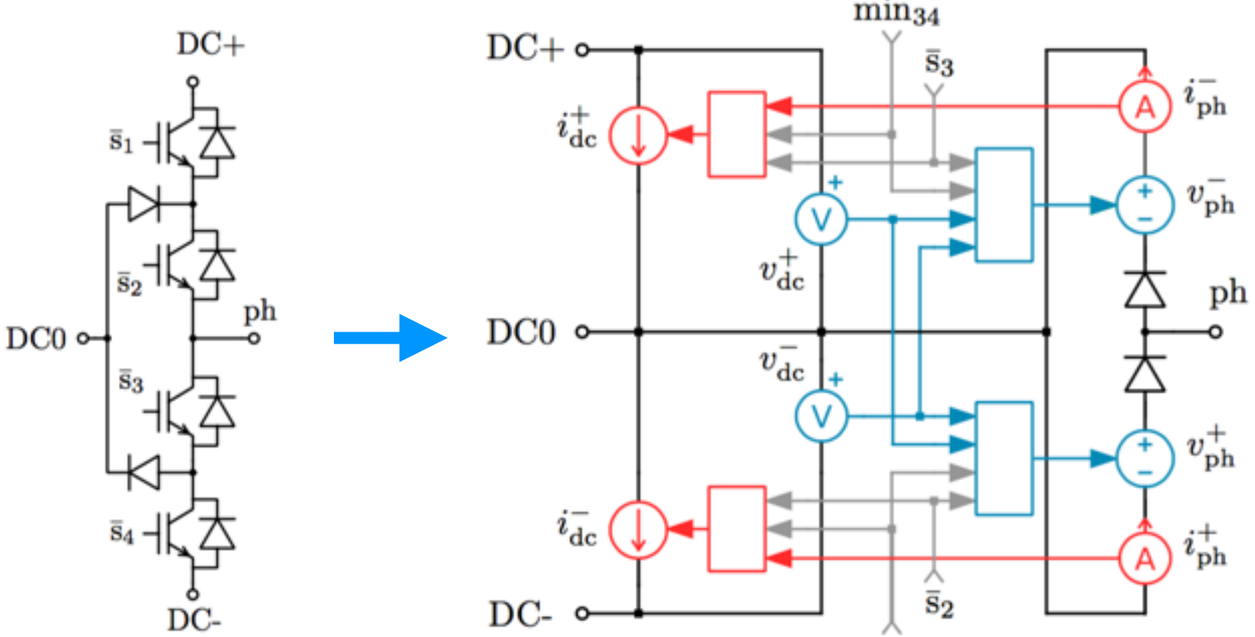
$$i_{dc}^+ = i_{ph}^+ \cdot \min_{12} - i_{ph}^- \cdot (1 - \bar{s}_3)$$

$$i_{dc}^- = i_{ph}^- \cdot \min_{34} - i_{ph}^+ \cdot (1 - \bar{s}_2)$$





Model with Sub-cycle Averaged Switching Signals (NPC)

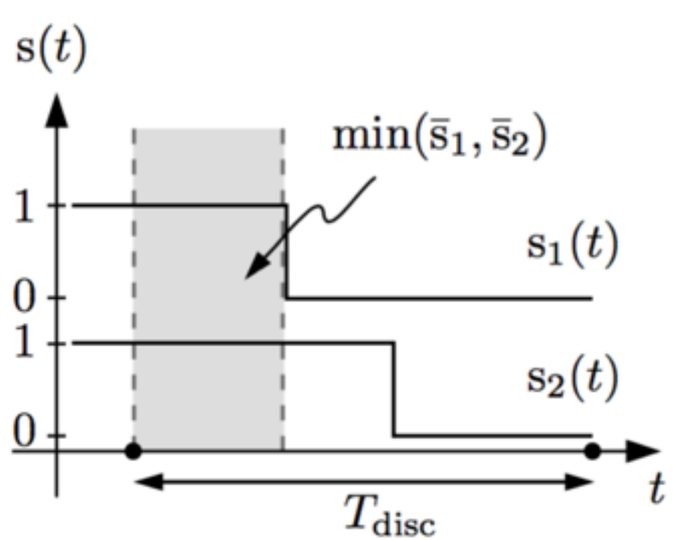


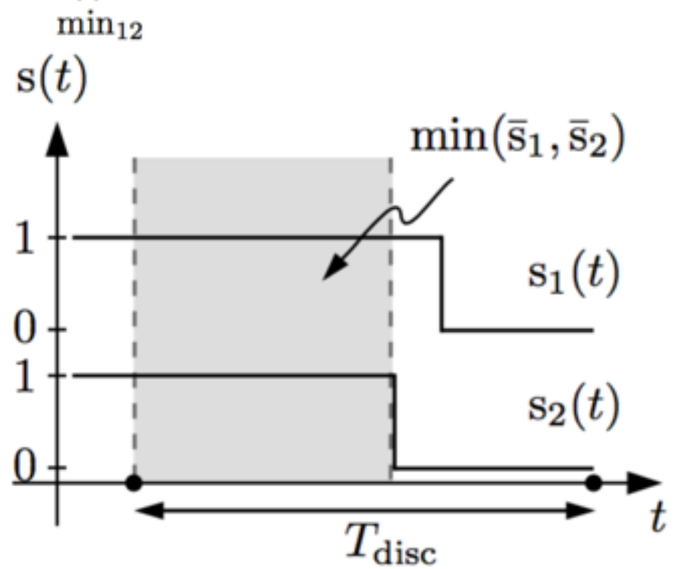
$$v_{ph}^+ = v_{dc}^+ \cdot \min_{12} - v_{dc}^- \cdot (1 - \bar{s}_2)$$

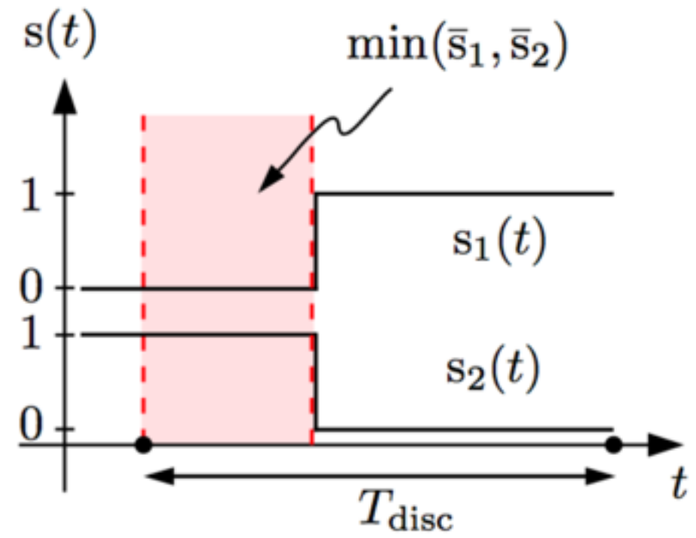
$$v_{ph}^- = v_{dc}^- \cdot \min_{34} - v_{dc}^+ \cdot (1 - \bar{s}_3)$$

$$i_{dc}^+ = i_{ph}^+ \cdot \min_{12} - i_{ph}^- \cdot (1 - \bar{s}_3)$$

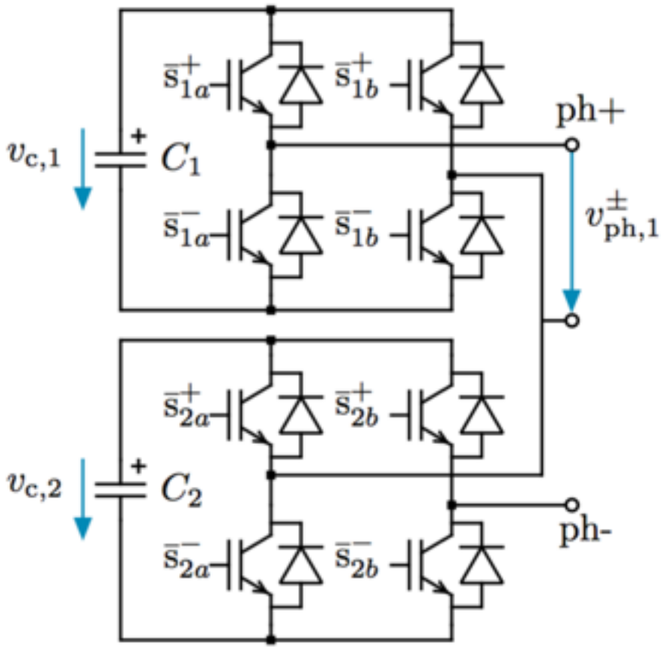
$$i_{dc}^- = i_{ph}^- \cdot \min_{34} - i_{ph}^+ \cdot (1 - \bar{s}_2)$$

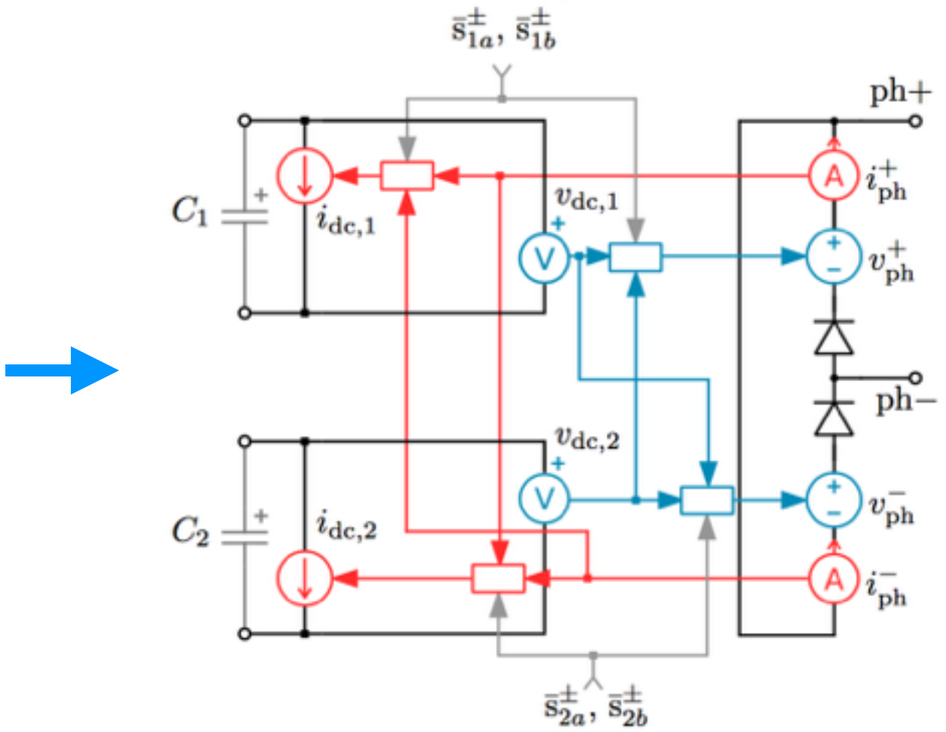






Model with Sub-cycle Averaged Switching Signals (CHB)





$$v^{+}_{\mathrm{ph}} = \sum_{\ell=1}^{n} v_{\mathrm{dc},\ell} \cdot (\bar{s}^{+}_{\ell a} + \bar{s}^{-}_{\ell b} - 1)$$

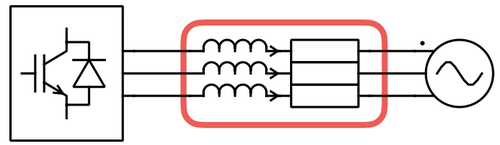
$$v^{-}_{\mathrm{ph}} = \sum_{\ell=1}^{n} v_{\mathrm{dc},\ell} \cdot (\bar{s}^{-}_{\ell a} + \bar{s}^{+}_{\ell b} - 1)$$

$$i_{\mathrm{dc},\ell} = (\bar{s}^{+}_{\ell a} + \bar{s}^{-}_{\ell b} - 1) \cdot i^{+}_{\mathrm{ph}} + (\bar{s}^{-}_{\ell a} + \bar{s}^{+}_{\ell b} - 1) \cdot i^{-}_{\mathrm{ph}}$$

Modeling of Converter Grid

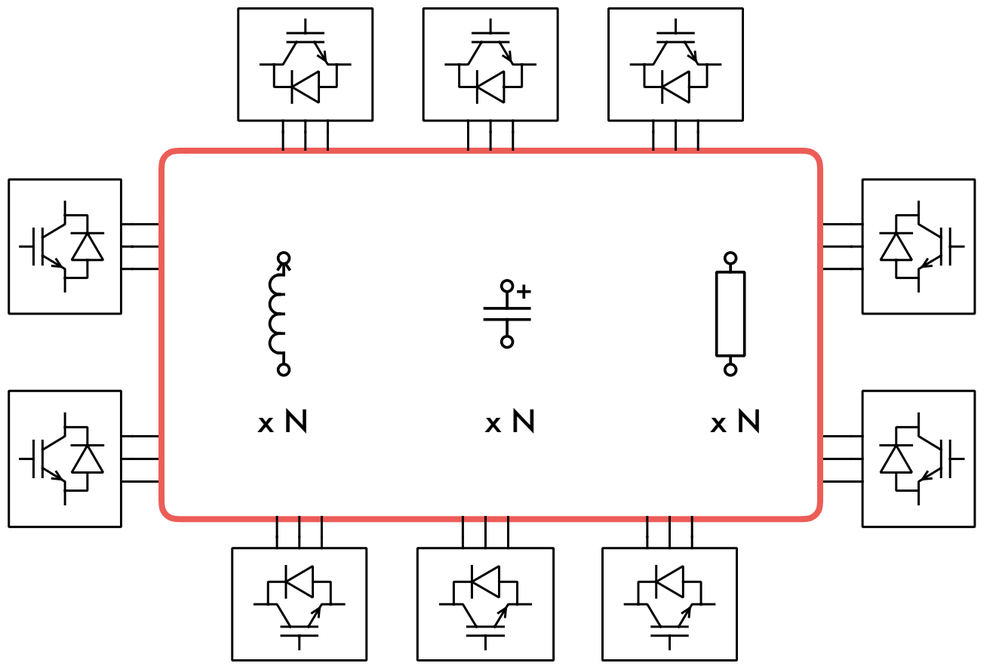
Simulation of a single converter

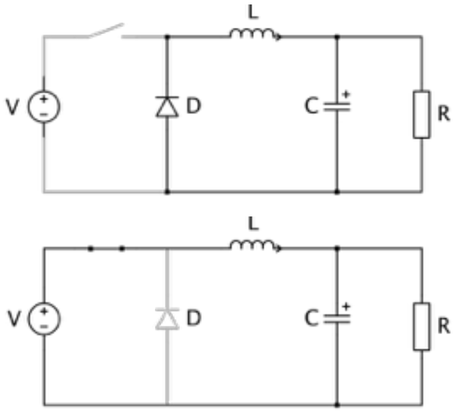
- Grid modelled simply as AC voltage source and impedance
- Low challenge for modern simulators for power electronics



Simulation of a grid with multiple converters

- Large number of switching components
- Leads to huge number of matrices
- Large number of passive components





$$A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \quad D = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

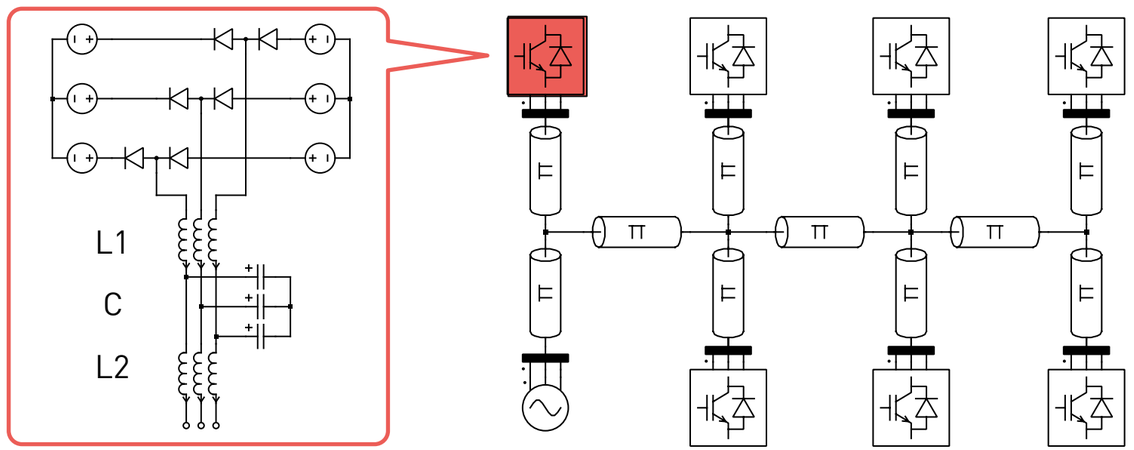
$$A = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \quad D = \begin{bmatrix} -1 \\ 0 \end{bmatrix}$$

System Partitioning

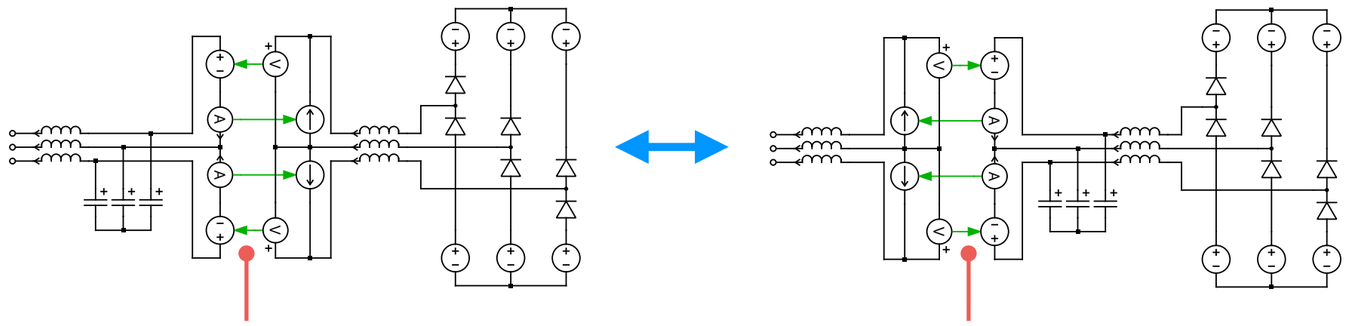
Large-scale circuit

- Original circuit: 7x6 switches
- Number of [A, B, C, D] 2^{42}



Capacitor voltage splitting

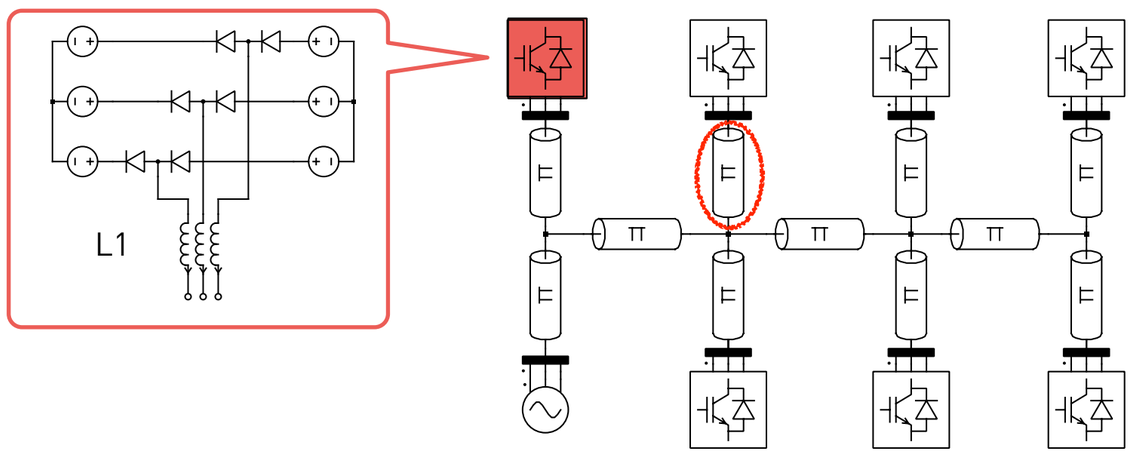
- Assuming converters have LCL filter
- Split the system at the filter capacitors
- Voltage applied on grid side
- Current applied on converter side
- Number of [A, B, C, D] $2^6 \times 7 + 1$
- C should be left on which side?



System Partitioning

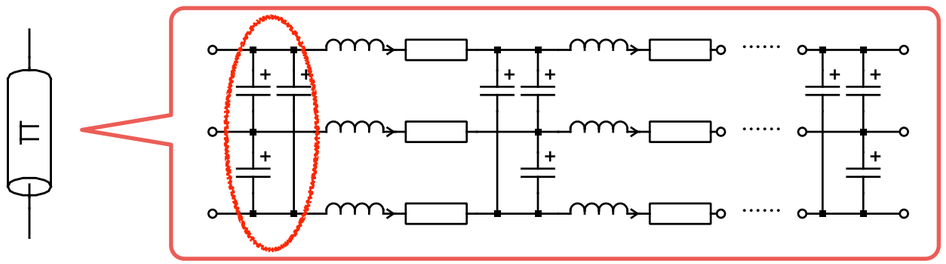
If only L filter installed

- Cable need to be modelled as Pi section
- Cable capacitance can be used for split
- Capacitor kept on the side with relatively smaller inductance
- To minimise the instability issue of the one model step delay



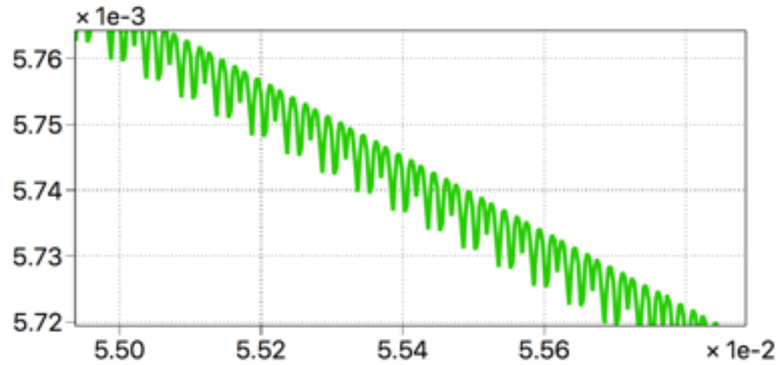
Take care about stiffness

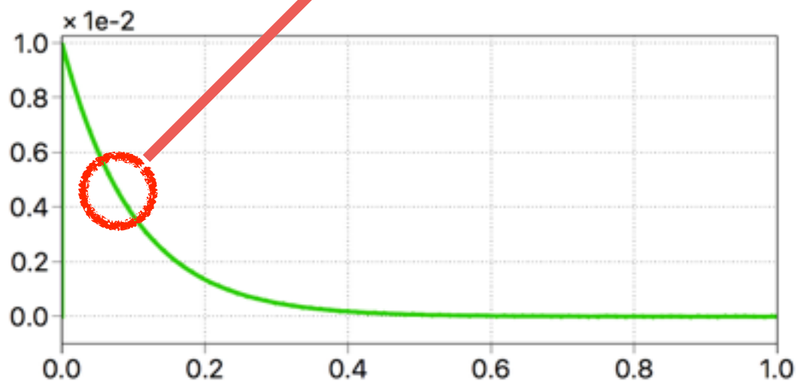
- Cable capacitances only modelled where necessary for splitting

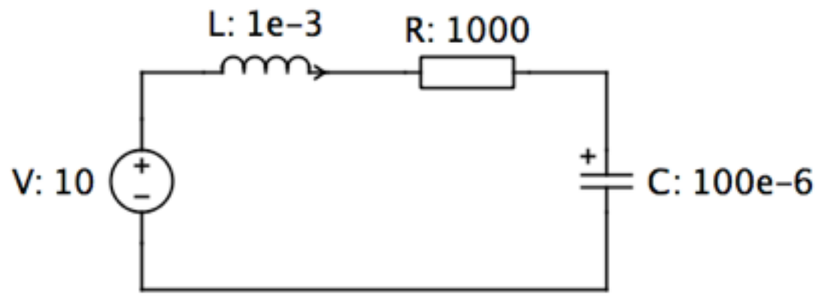


Example of Stiff System

- Eigenvalues of this simple circuit are orders of magnitude apart





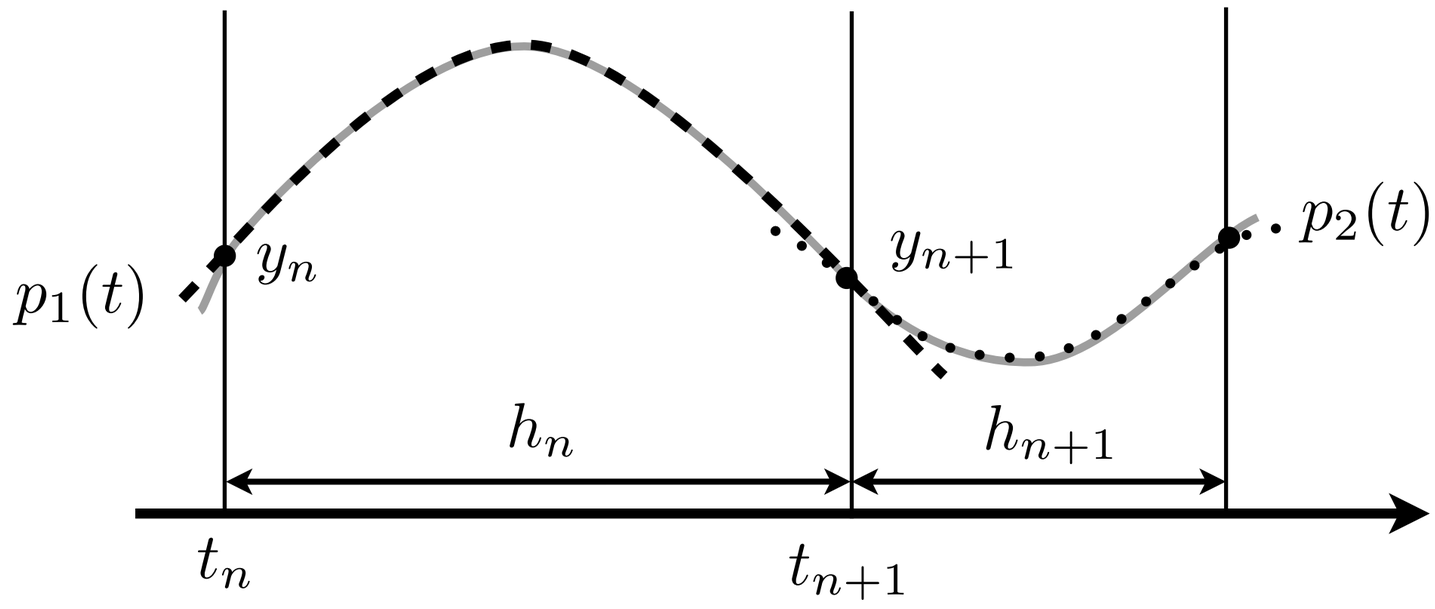


$$\lambda_{1,2} = -\frac{R}{2L} \pm \frac{1}{2}\sqrt{\frac{R^2}{L^2} - \frac{4}{LC}}$$

$$\begin{aligned} \lambda_1 &\approx -99999 \\ \lambda_2 &\approx -10 \end{aligned}$$

Continuous Solver Operation

- y(t) can be constructed using in a piecewise fashion using $p_1(t)$ and $p_2(t)$, which are Taylor series polynomials
- A continuous solver calculates the point y_{n+1} by calculating the equivalent Taylor series for $p_1(t)$
- An n^{th} order solver has the same accuracy as an n^{th} order Taylor series

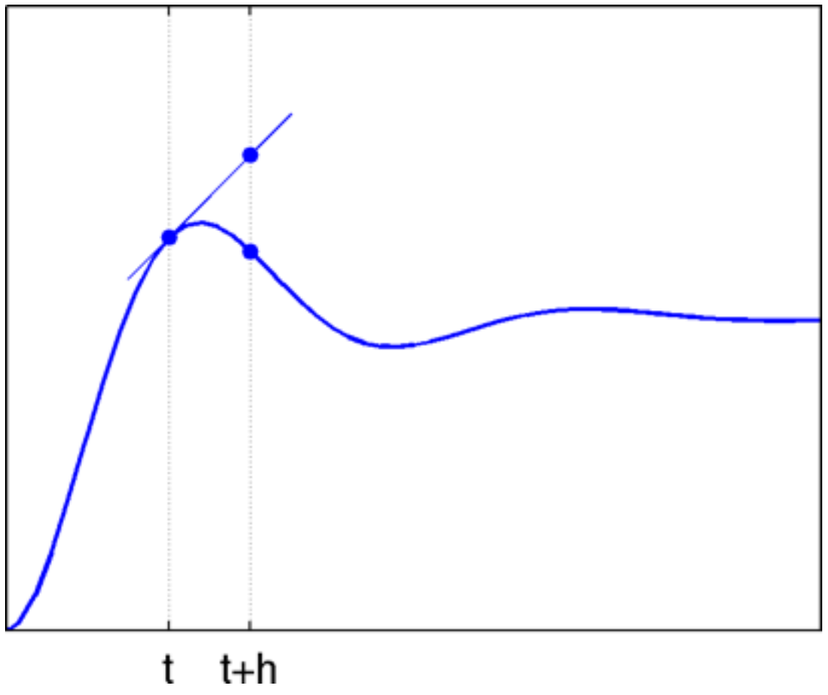


Forward Euler

- Truncate the Taylor Series after the first term:

$$\boldsymbol{x}(t^* + h) \approx \boldsymbol{x}(t^*) + \boldsymbol{f}(\boldsymbol{x}(t^*), t^*) \cdot h$$

$$\boldsymbol{x}_{k+1} = \boldsymbol{x}_k + \boldsymbol{f}(\boldsymbol{x}_k, t_k) \cdot h$$



- 1st order accurate

- Explicit integration algorithm

Numerical Experiment

- Scalar system

$$\dot{x} = a \cdot x$$

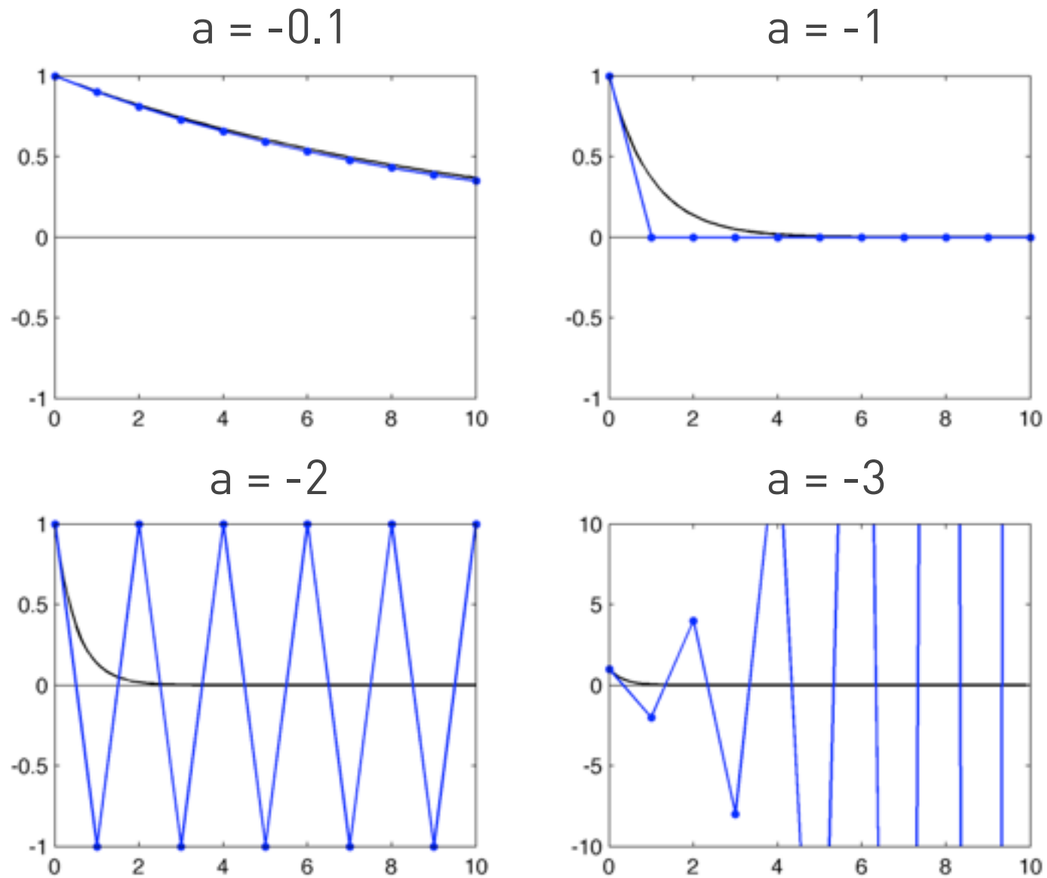
- Analytical solution

$$x(t) = x_0 \cdot e^{a \cdot t}$$

- Use ‘our’ Forward Euler

$$\begin{aligned} x_{k+1} &= x_k + ah \cdot x_k \\ &= (1 + ah) \cdot x_k \\ x_k &= x_0 \cdot (1 + ah)^k \end{aligned}$$

- Unstable for a < -2



Stability Analysis

- Autonomous LTI system

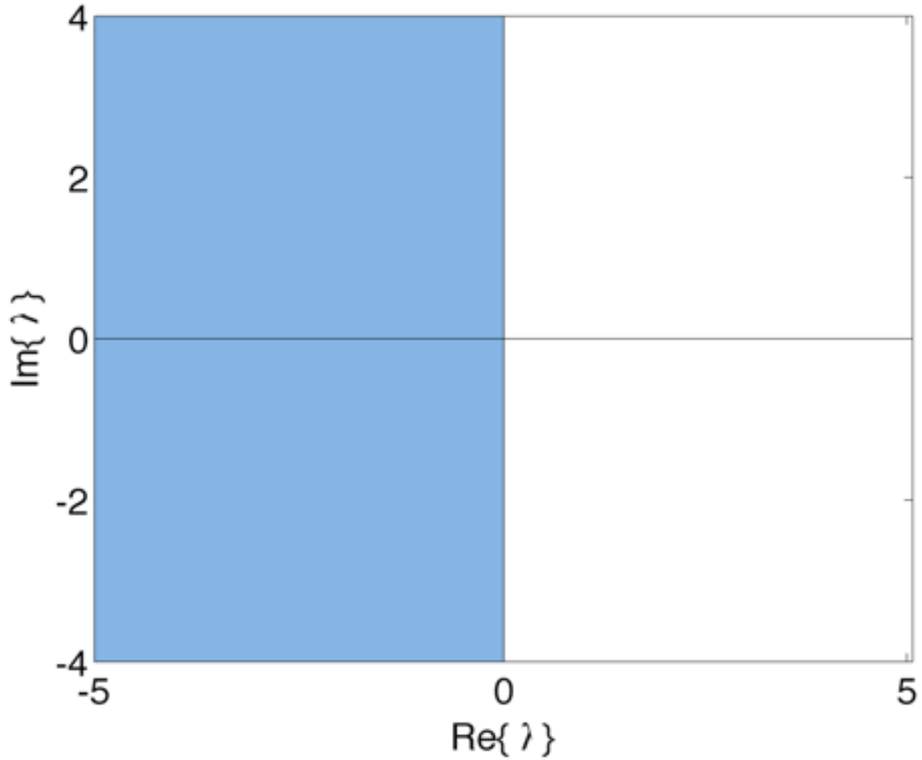
$$\dot{\boldsymbol{x}} = \boldsymbol{A} \cdot \boldsymbol{x}$$

- Analytical solution

$$\boldsymbol{x}(t) = \boldsymbol{x_0} \cdot e^{\boldsymbol{A} \cdot t}$$

- Analytically stable if

$$\mathrm{Re}\{\mathrm{Eig}(\boldsymbol{A})\} = \mathrm{Re}\{\lambda\} < 0$$



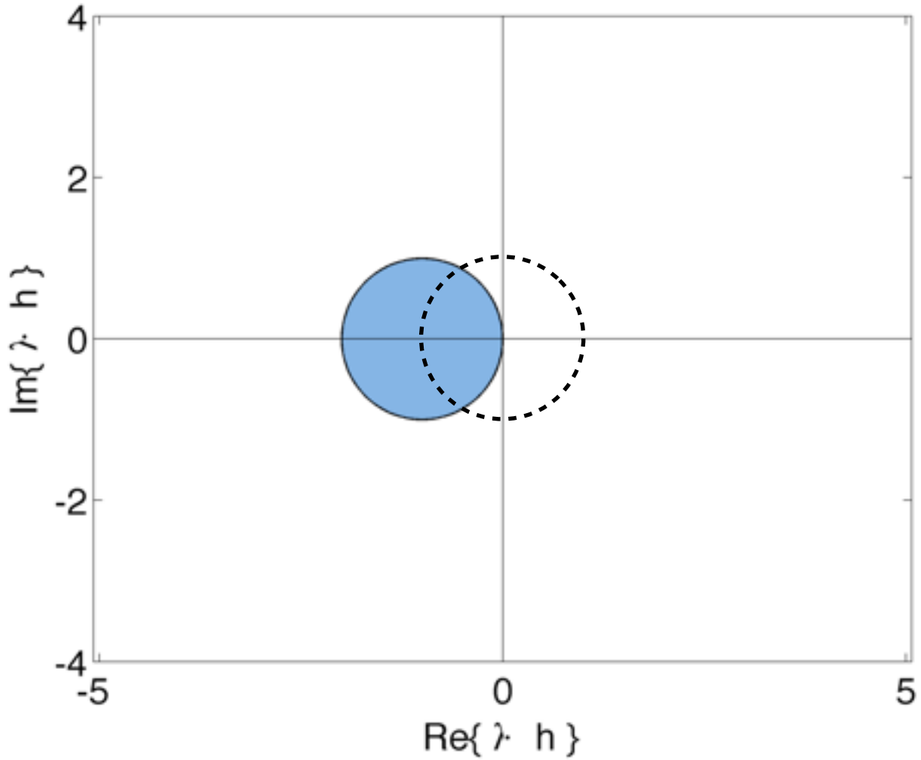
Stability Domain of Forward Euler

Integration algorithm

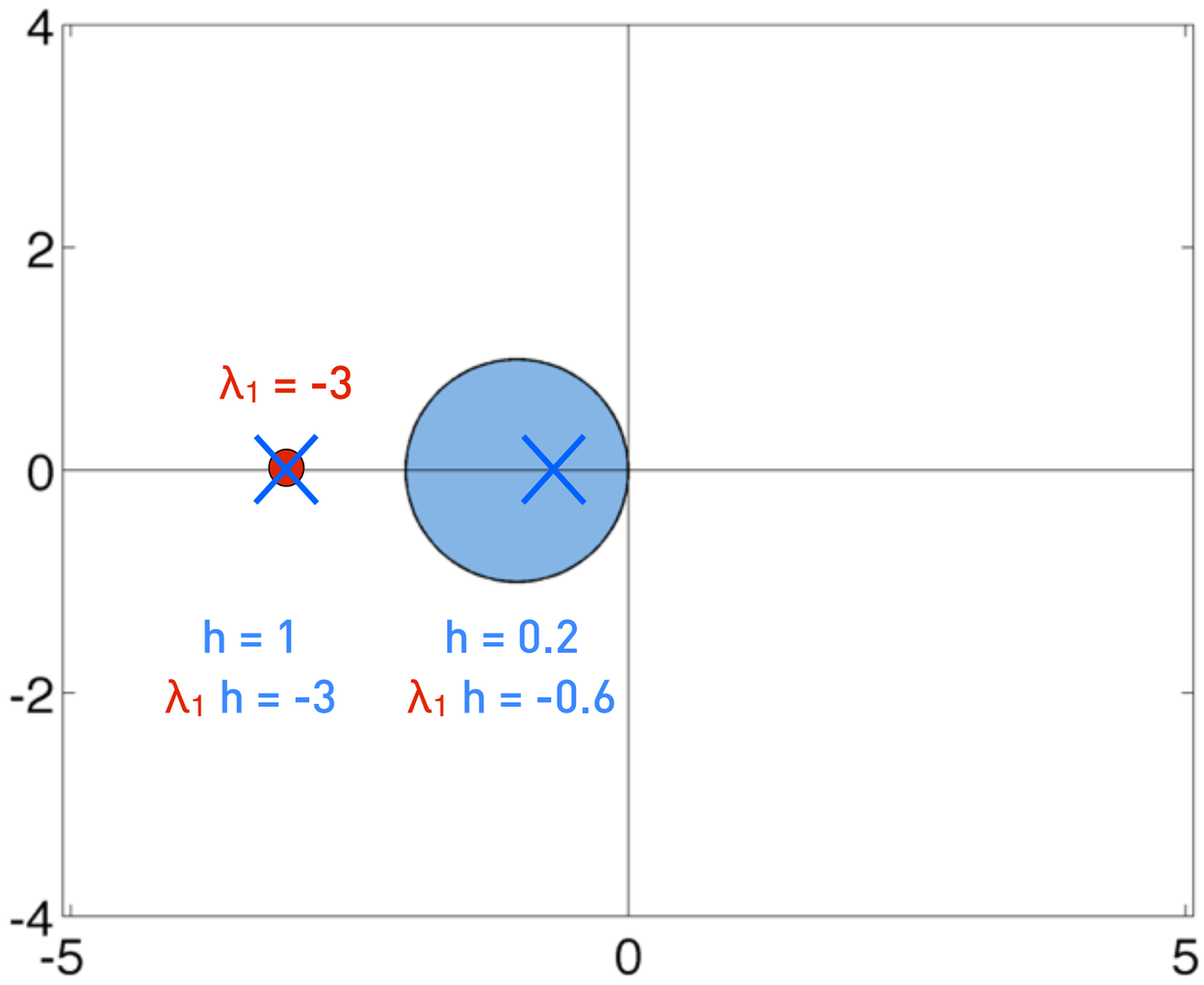
$$\begin{aligned} \boldsymbol{x}(t^* + h) &= \boldsymbol{x}(t^*) + \dot{\boldsymbol{x}}(t^*) \cdot h \\ &= \boldsymbol{x}(t^*) + \boldsymbol{A} \cdot h \cdot \boldsymbol{x}(t^*) \end{aligned}$$

$$\begin{aligned} \boldsymbol{x}_{k+1} &= (\boldsymbol{I} + \boldsymbol{A} \cdot h) \cdot \boldsymbol{x}_k \\ &= \boldsymbol{F} \cdot \boldsymbol{x}_k \end{aligned}$$

- Stable if the eigenvalues of $\boldsymbol{F}$ are inside the unit circle (0,0)
- Therefore if the eigenvalues of $\boldsymbol{Ah}$ are inside a unit circle around (-1, 0)

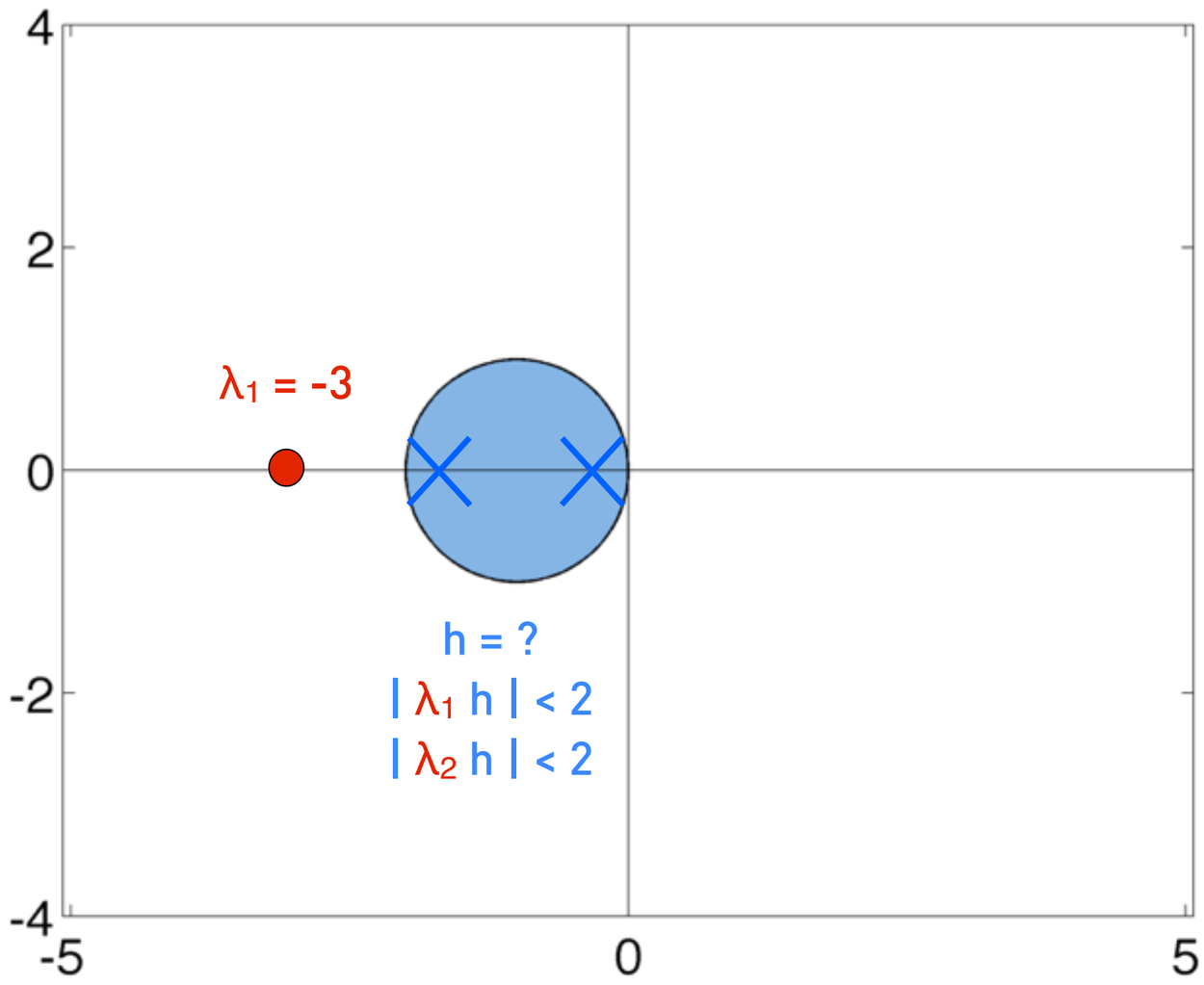


Stability Domain of Forward Euler



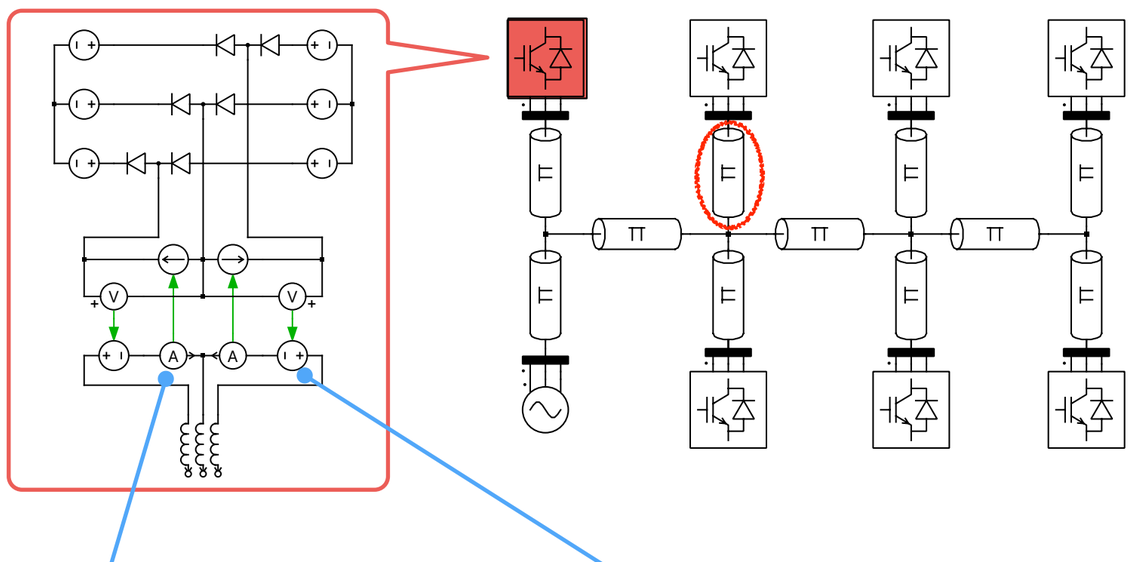
Stability Domain of Forward Euler

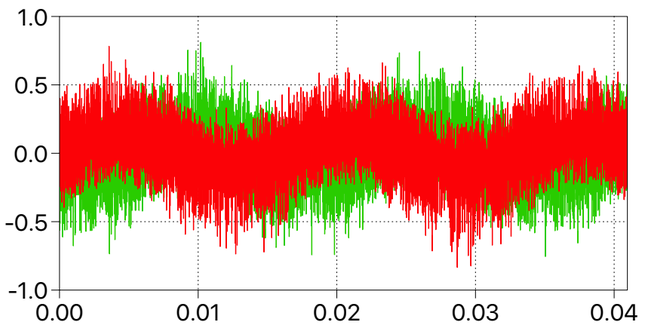
$\lambda_2 = -10000$

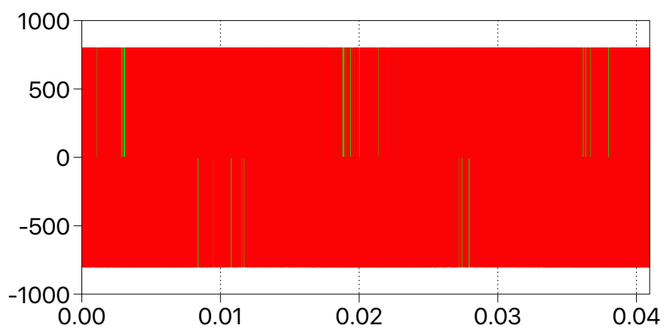


System Partitioning

- To avoid the delay in the grid
  - Split the model directly at VSI output
  - Current source at the VSI output
  - Voltage source at the grid side
- Works in active state
- Inactive state (free wheeling)
  - Small oscillation on output current
  - Pulsed voltage on the VSI output
  - Voltage source can not represent OC
  - Cable capacitance need to be modelled
  - Prevent the high frequency pulse voltage penetrate further into grid







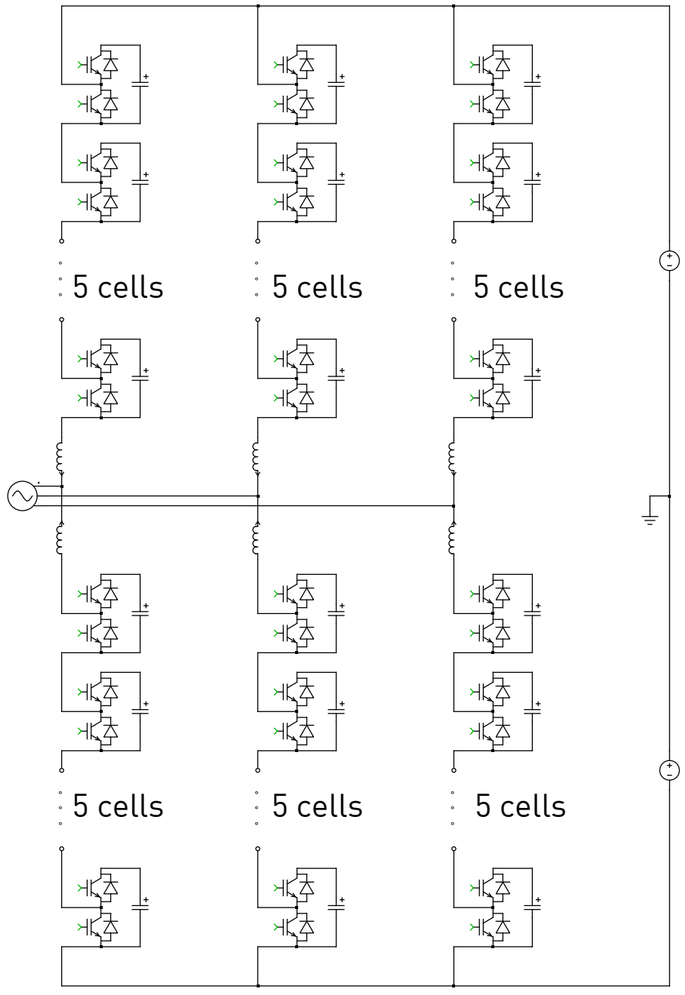
Model Partitioning

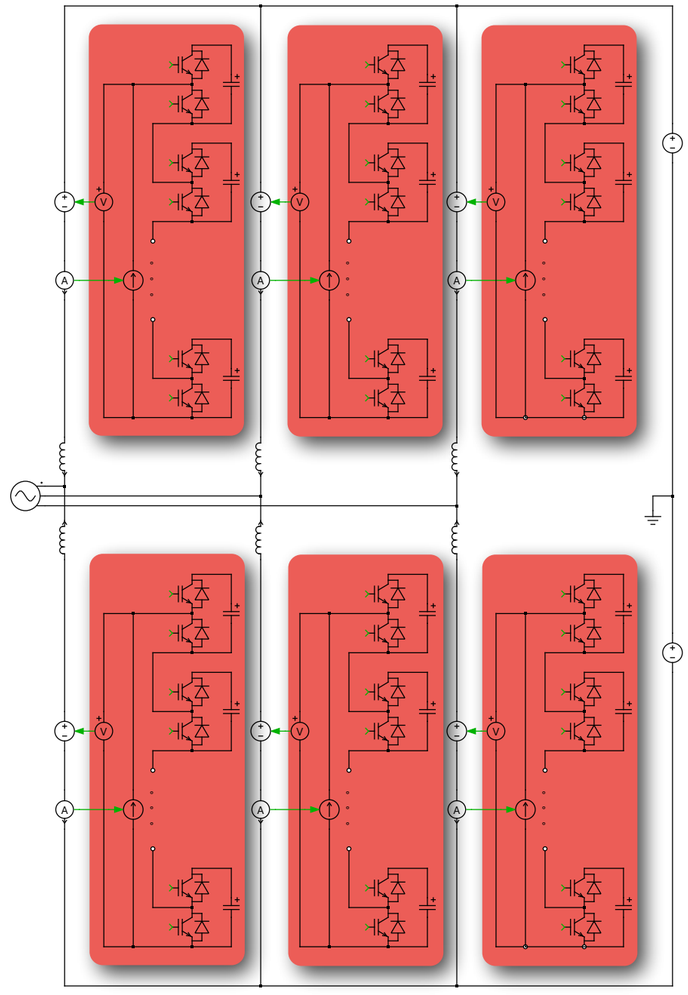
MMC or CHB

- Original circuit: 10x6 switches
- Cells using module: 2x6 switches
- Number of combinations 2^{12}

Inductive current splitting

- Split the system on the inductor
- Inductor kept on grid side
- Voltage applied on grid side
- Current applied on module side
- Number of combinations $2^2 \times 6$



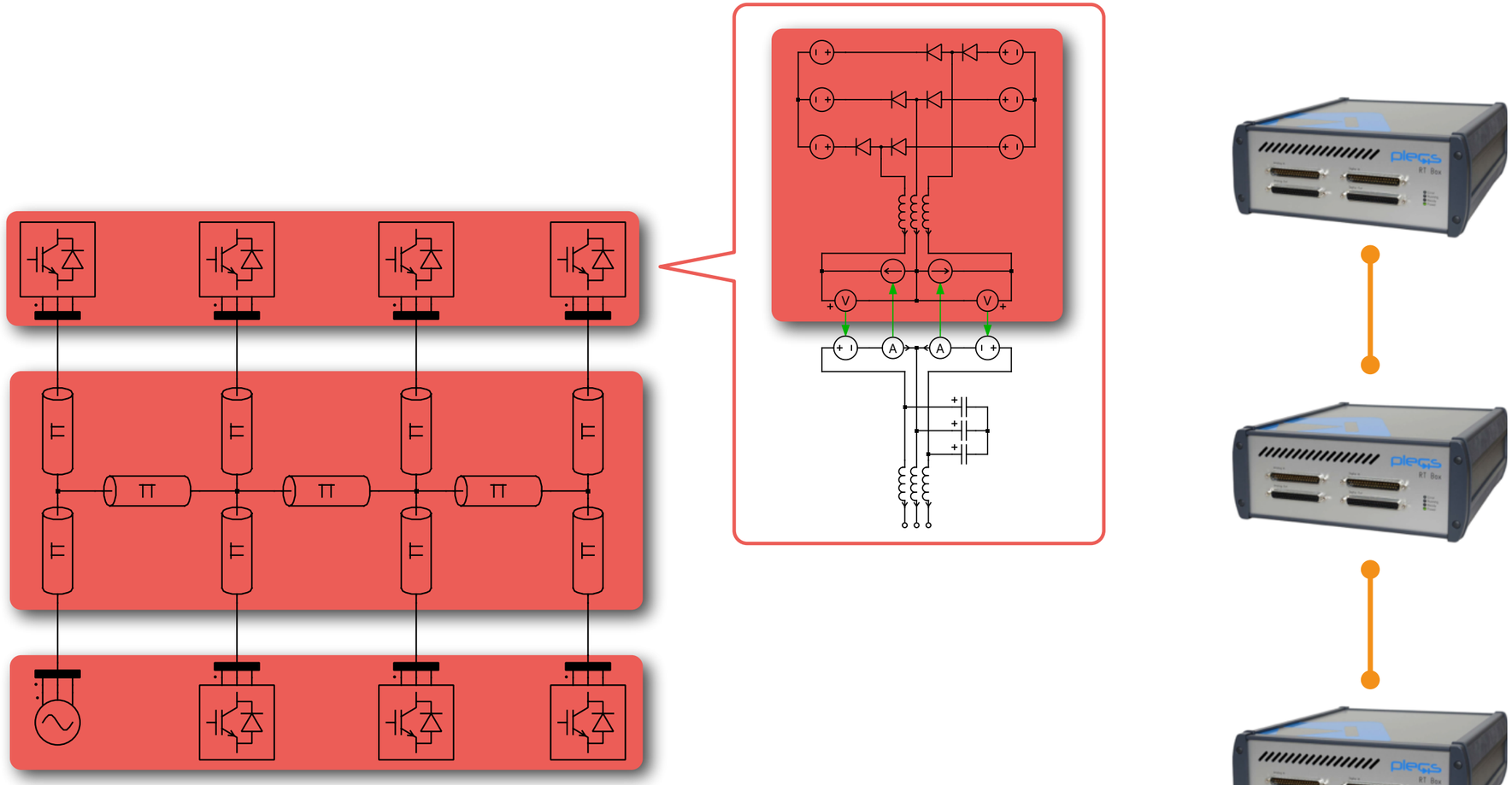


Interconnection

- SFP interface
- Electrical- or optical link
- Aurora protocol

Parallel Computation

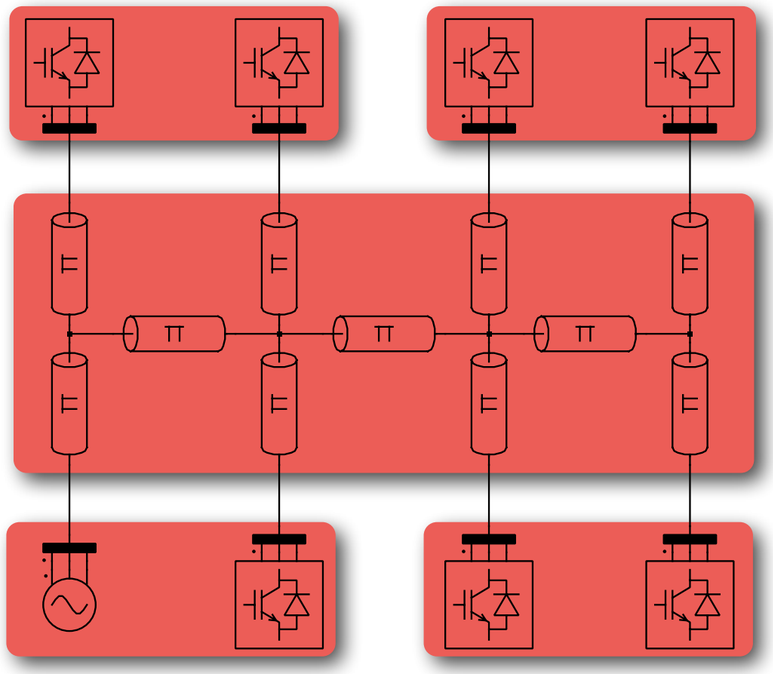
Split the converters from the grid

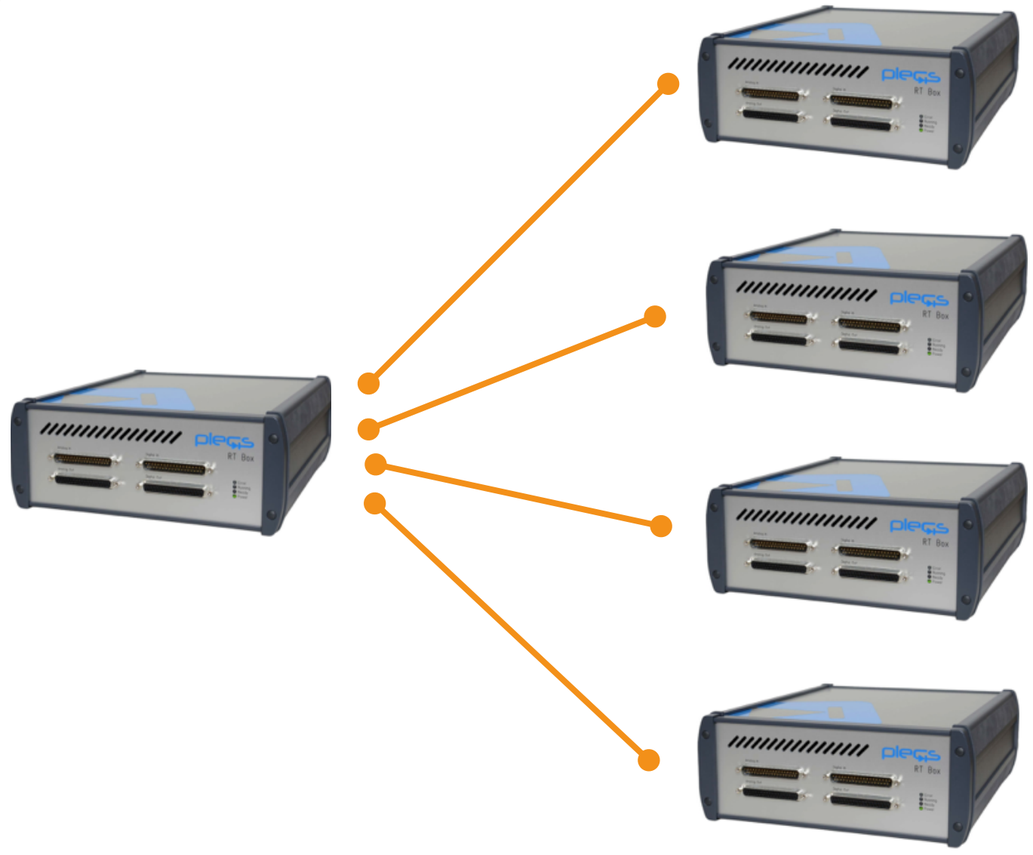


Parallel Computation

Split the converters from the grid

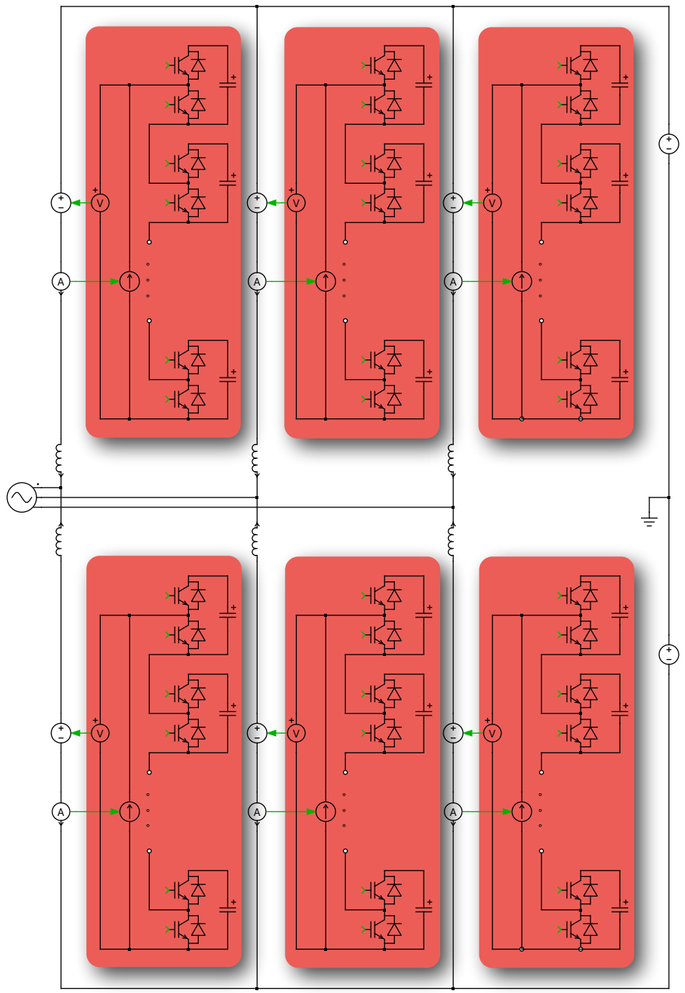
- Reduce model step size of the power converters
- Try to keep tree connection to reduce delay

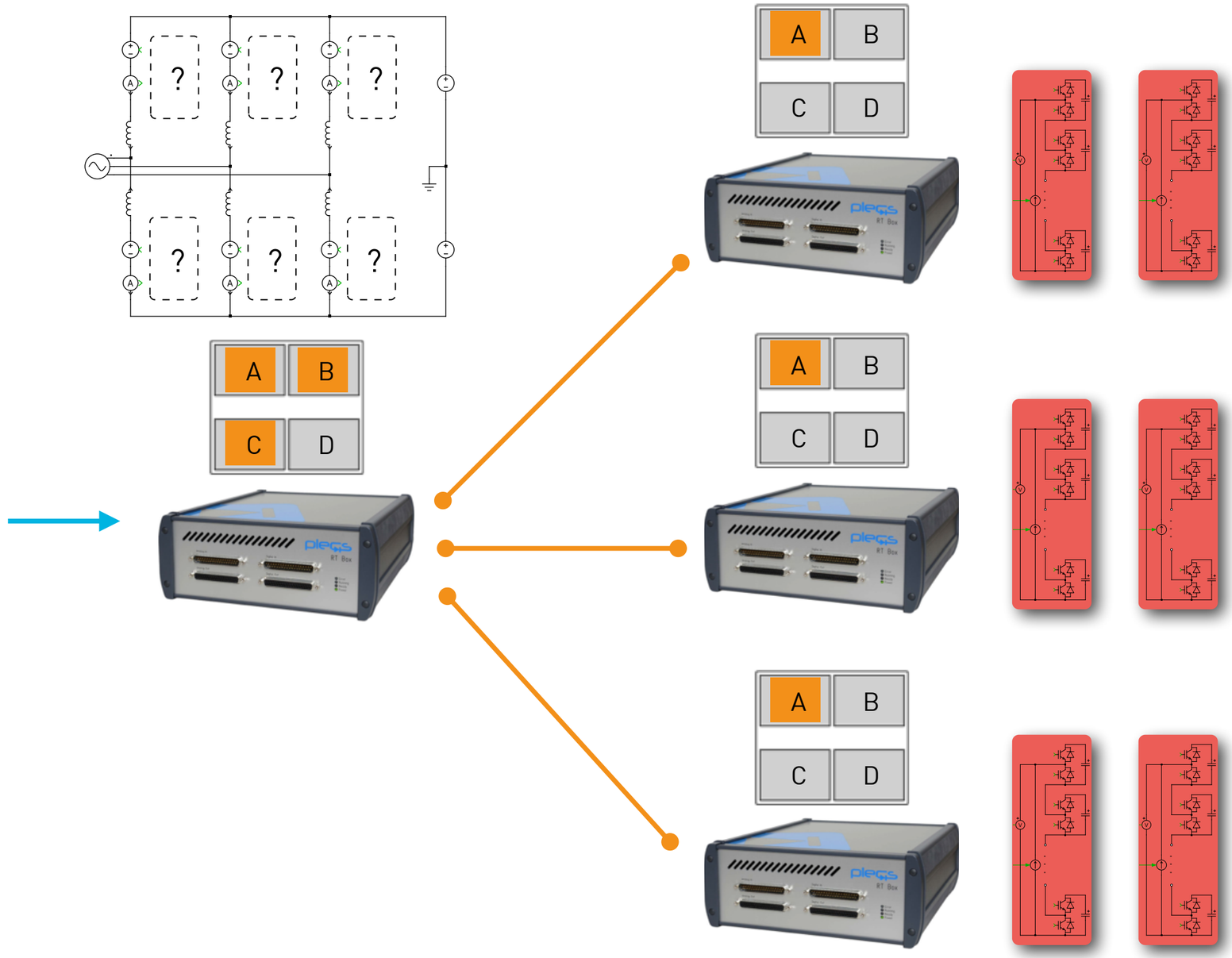




Parallel Computation

Split MMC or CHB

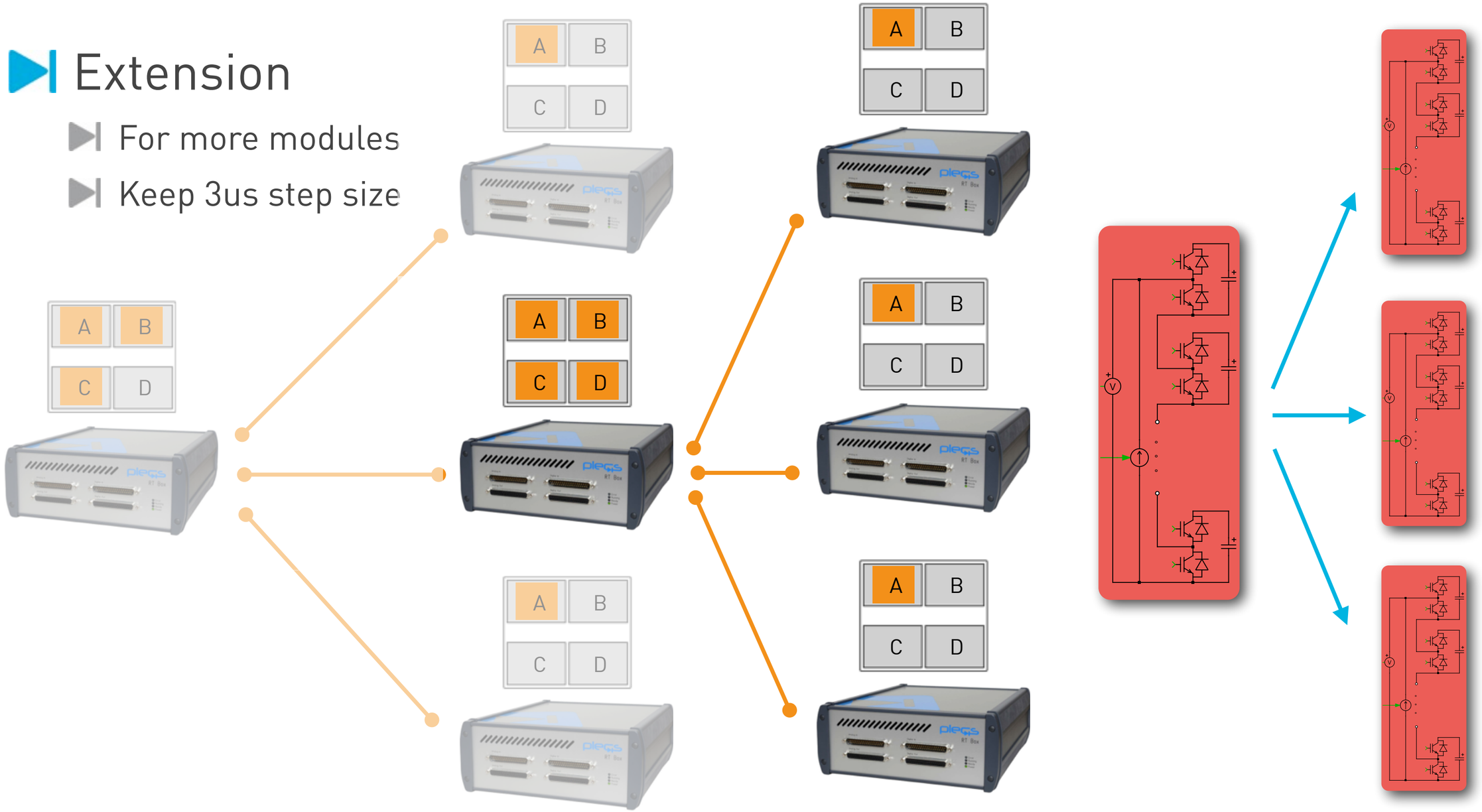




Parallel Computation

Extension

- For more modules
- Keep 3us step size



electrical engineering software

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